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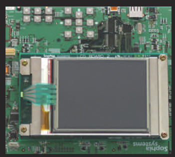

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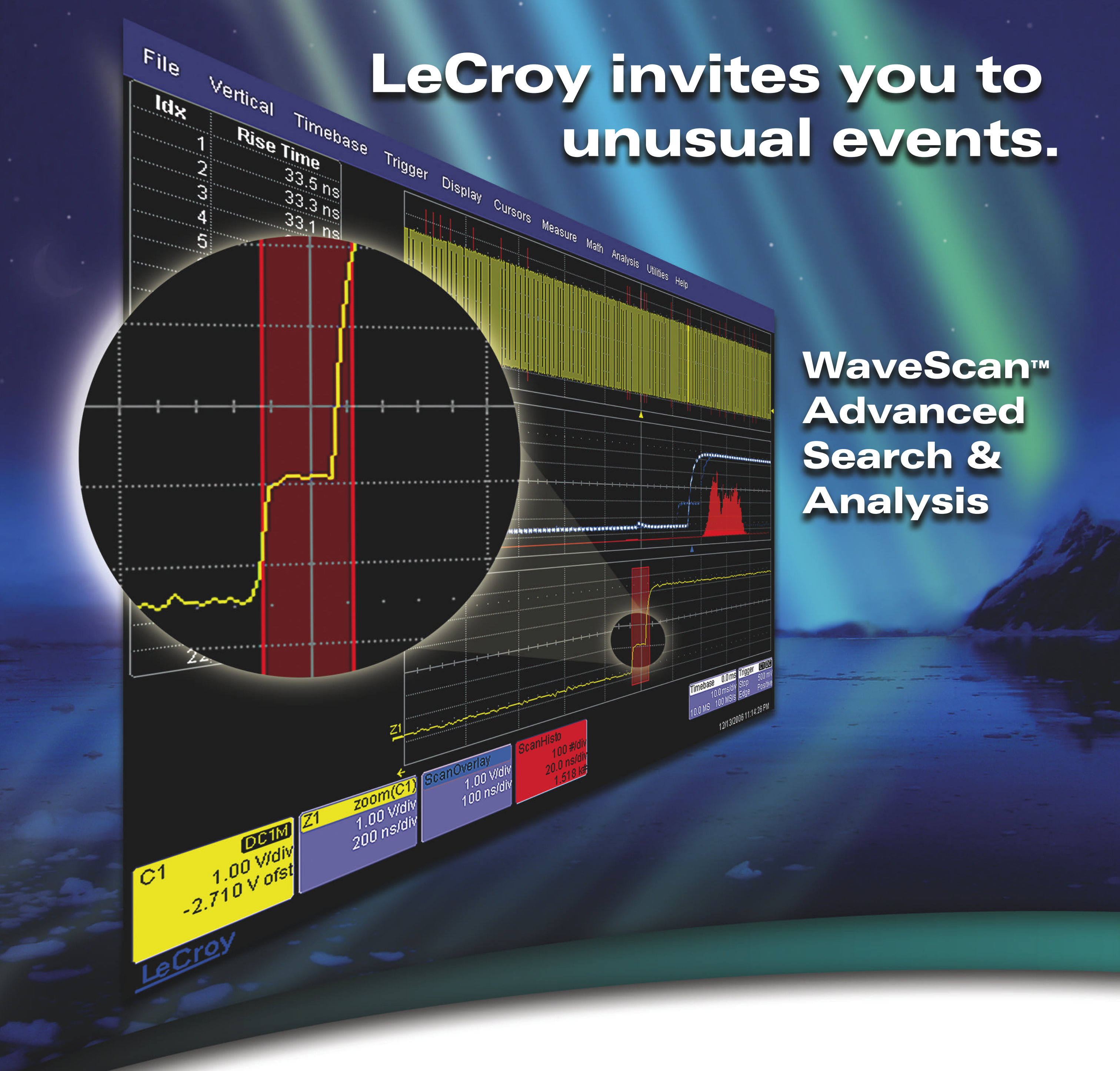

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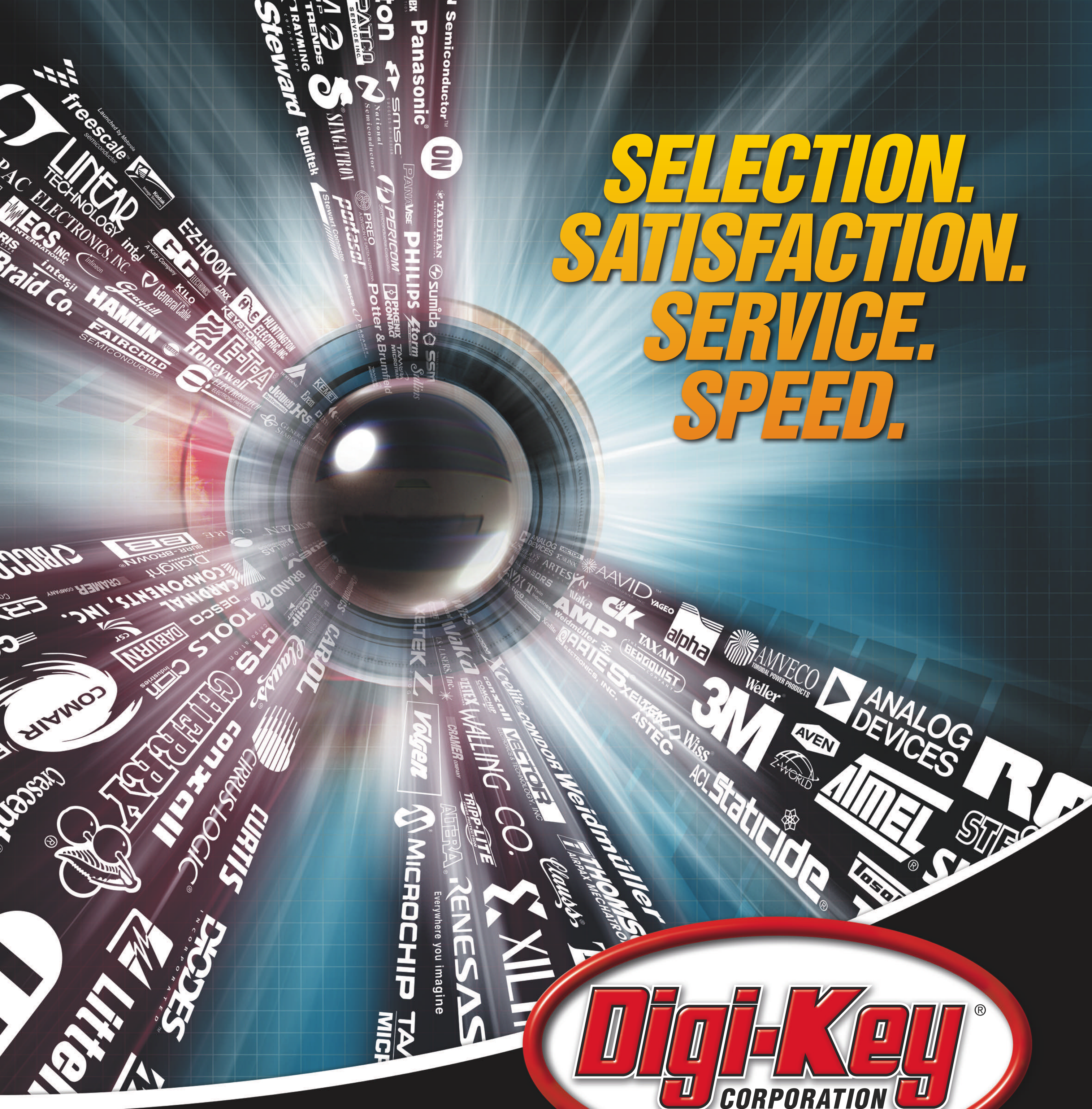
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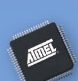

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Addressing The Design Challenges Facing Today's Smartphone Architects

By: QUICKLOGIC®

▶THE SITUATION

Today the communications industry is riding a wave of achievement, prompted by recent developments in wireless standards and technology, product announcements hailing feature-rich content and new functionality, and ongoing research and development. Nowhere is this achievement more apparent than with the Smartphone. According to Gartner research analysts, Smartphone sales increased 75.5 percent in 2005 to 37.4 million units and grew a further 66 percent in 2006. Driven in part by increased integration of applications and features, this growth is not expected to let up anytime soon.

While the integration — with its flexibility and versatility to meet a wide range of consumer needs — creates new opportunities, it also leads to a number of challenges, not the least of which is the increased risk that results from consumer volatility. Which applications and features are likely to be integrated to satisfy consumer needs? More importantly, how will these standards-based applications and features be added, or connected, to the device processors given that they typically don't talk to one another?

System-level engineers and, in particular, system architects sit on the front line of the Smartphone development process. It is their job to balance the complexity of creating Smartphones with the new and emerging applications and features that consumers demand. In doing so, they must confront this connectivity challenge without sacrificing battery life, board space, cost, and product schedule.

▶CHALLENGES

Today's system architects face a litany of challenges, such as support for new standards, and adding more features without increasing costs, size and power consumption. How well engineers deal with these challenges may ultimately be the decisive factor in whether or not the end products they design secure a lasting competitive advantage in the industry.

▶CONSIDERATIONS

System architects facing these challenges are often forced to make tough architectural decisions, early in the design process. If made incorrectly, these decisions can adversely impact things such as area, cost and time to market.

Whether designing a Smartphone or other mobile device, there is specific functionality that system architects now require when making these architectural decisions. This functionality includes:

• Integrated Platform
Applications such as Voice over IP (VoIP), Web surfing, and MP3 and movie play back are today some of the most desirable convergent applications to implement into consumer electronic devices like the Smartphone. For VoIP and Web surfing, Wi-Fi is a must have. For MP3 and movie play back, adding larger amounts of storage are required. Easily adopting these technologies into the Smartphone requires an integrated solution which not only helps replace discrete components, but can also act as a seamless interface for different processors.

• Flexibility (e.g. adaptability or ability to customize)
When designing Smartphones, system architects require a solution with the flexibility to implement complex mature interfaces as well as custom functions. Without this functionality, the solution would not be able to quickly make changes to connect new standards, and avoid costly custom ASIC costs.

• Low Power
With a Smartphone, or other mobile devices, power consumption is a key consideration. It is imperative that standby power and dynamic power consumption be reduced in order to increase battery life.

PROFILE QuickLogic Corporation

QuickLogic Corporation NASDAQ: QUIK) is the leading provider of the lowest power programmable solutions for the portable electronics, industrial, communications and military markets. Our latest products, ArcticLink™, PolarPro™, Eclipse II™ and QuickPCI™ are being used to implement bridge and control solutions in embedded systems requiring Wi-Fi, DVB-H and IDE or CE-ATA-based disk drives. QuickLogic's proprietary ViaLink® technology offers significant benefits for programmable logic, including the lowest power, instant on capability and unmatched intellectual property security. The company is located at 1277 Orleans Drive, Sunnyvale, CA 94089-1138. www.quicklogic.com

▶THE SOLUTION

Specifically designed for mobile devices like the Smartphone, the ArcticLink Solution Platform from QuickLogic is an integrated and flexible connectivity platform which combines the benefits of low-cost, low power gate array technology with the flexibility of low power programmable fabric to address the time-to-market and R&D spending pressures which now dominate the consumer market. Unlike other commercially-available devices, ArcticLink delivers all the functionality system architects require today to give them, and the products they create, a heads up against the competition.

The ArcticLink family of devices consists of hardwired building blocks, such as the single-port Hi-Speed USB 2.0 OTG, SD/SDIO/MMC/ATA host controllers, and an embedded ultra-low power programmable fabric block, all in a single-chip solution (see *Figure 1*). A combination of small form factor packaging, ultra-low power technology and host bus interface configurability makes this highly integrated platform ideal for addressing emerging connectivity requirements in power-critical mobile applications.

ArcticLink's programmable fabric supports a range of available interfaces like PCI, IDE, NAND Flash, Managed NAND and Solid State Drives, SDIO and SPI, Hi-Speed UART, and ULPI-based (PHY-less) USB system interconnects. Through this fabric, the host bus interface can be tailored to expand the peripheral set of a broad variety of common mobile application processor families (e.g., processors with a multiplexed or de-multiplexed local bus) to meet the emerging connectivity requirements for wired/wireless communications and media storage. ArcticLink's internal split bus architecture supports sustained and concurrent data transfers, between slow- and high-speed peripherals, and to/from the common programmable fabric-based host interface.

The ArcticLink platform boasts a number of key advantages, including:

• Integrated Platform
As a highly integrated connectivity solution platform, ArcticLink effectively brings together on a single chip the Hi-Speed USB 2.0 OTG with built-in PHY, Hi-Speed SDIO host controller, multi-format storage interface (e.g., SD, MMC, Managed NAND, or CE-ATA) and programmable solutions in fabric. This level of integration enables the replacement of up to 5 discrete components in a mobile device. The result is a significantly lower BOM cost and board space savings.

• Flexibility
As a highly flexible platform, ArcticLink features configurable host controller and storage solutions. Its user-programmable fabric enables custom functions as well as additional tested, proven solutions from QuickLogic (including software driver, reference schematic, etc.) to be easily and seamlessly interfaced as well. This flexibility avoids costly custom ASIC costs as new standards emerge or change.

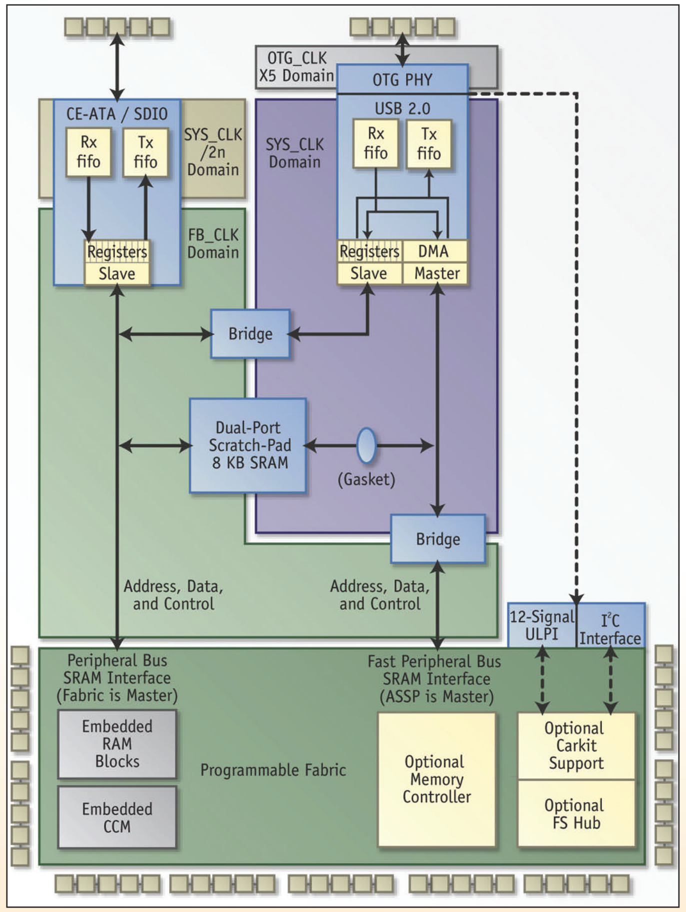

Figure 1. ArcticLink Architecture Block Diagram.

• Low Power
Designed for mobile devices, ArcticLink features a low-power hard-wired implementation for complex USB and SDIO controllers, the industry's lowest power programmable fabric and a Very-Low-Power mode to put devices in sleep mode. The higher performance and power management afforded by these capabilities saves energy, while a built-in DMA engine offloads the CPU from heavy data manipulation and transfer; further minimizing power consumption.

ArcticLink's highly-integrated nature, coupled with its cost effectiveness, energy efficiency and flexibility offer today's system architects everything they need to accelerate time-to-market and effectively solve today's connectivity challenge. ■

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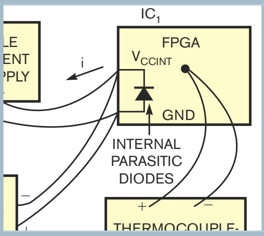

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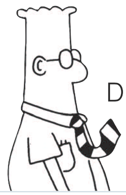

DEPARTMENTS & COLUMNS

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BY MAURY WRIGHT, EDITOR IN CHIEF

Innovation winners span analog ICs to EDA

On Monday, April 2, in San Jose, CA, *EDN* again honored the most innovative products and engineers at the 17th rendition of the *EDN* Innovation Awards. As always, we had an outstanding set of nominees. I appreciate the diligent work of the *EDN* staff in selecting finalists. And thanks to all of the readers and the *EDN* Editorial Advisory Board members that voted. You will find the full list of winners on pg 53.

I'd like to highlight a few of the winners here and spotlight how the winners match industry trends and map to trends in consumer products. Without a doubt, consumers buying digital-media products are now directly driving the tech industry. The PC is still vitally important, although the PC now arguably fits into the consumer category. The communication segment also remains key, but remember: Those digital consumer products drive much of the market growth in communications. Even segments such as automotive these days include a tremendous amount of digital-media technology.

The best example of enabling technology matching the digital-media trend came in the new category of mixed-signal ASSPs (application-specific standard products). In the past, we've force-fit these types of products into one of the other digital categories or into the broad analog-IC category.

The mixed-signal category included a motor controller from International Rectifier that cuts energy use and boosts efficiency in white goods, a software-driven radio from Cambridge Silicon Radio that supports Bluetooth and FM operation, and a miniature microphone from Akustica that delivers a digital output. All creatively mix the analog interface to the real world with digital circuits that simplify end-product design and improve the product. The winner, the Akustica digital MEMS (microelectromechanical) microphone, will find use in a variety of products ranging from mobile handsets, to audio recorders, to PDAs.

Every year, we have a broad set of EDA entries. The toughest challenge is always splitting the large number of entries into categories in which the products are somewhat comparable. It's not a perfect science, but Berkeley Design Automation's SPICE program in the front-end-IC category and Cadence's space-based router in the back-end-IC category are both vital in designing for the digital-media world.

I certainly don't want to minimize the importance of pure-digital technologies. Intel did perhaps its best work in more than a decade with the Core 2 Duo processor. The behemoth may have taken awhile to embrace lower clock speeds and multiple cores. But Intel looks to have hit a home run with its new architecture. We're also witnessing the emergence of the DSC (digital-signal controller) as a new class of processor that melds DSP and traditional processor architectures. Texas Instruments offers a prime example with its winning entry in the microcontrollers and DSCs category.

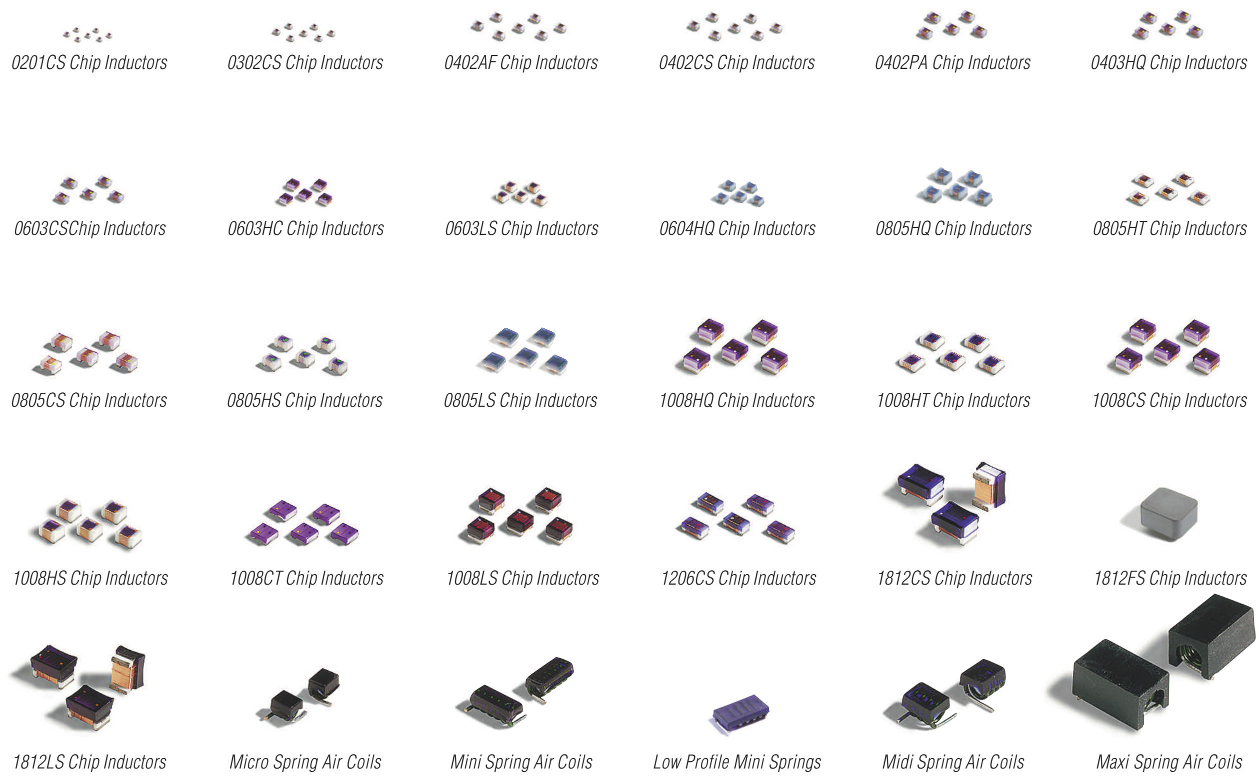
Plenty of other enablers of digital-media products are on the winners list, as well as the Agilent Medalist bead-probe technology, which enables testing of complex ICs for compelling end products. Winners include Freescale's Class D audio IC and video-codec technology from LSI Logic.

Ironically, however, the Innovator of the Year and the winner in the broad digital-IC category don't at first glance appear to fit the digital-media mold. I beg to differ. Xilinx took on a huge range of challenges, from moving to 65-nm-process technology to finding the right mix of programmability and hard-wired intellectual property in the Virtex-5 LXT FPGA design. Despite the move to a presumably leakier process node, the design yielded a 35% reduction in dynamic power consumption relative to 90-nm designs.

The Innovator of the Year award went to Xilinx's Steve Douglass, Suresh Menon, and their team of more than 200 engineers around the globe. Join me in congratulating the entire team and their dedication to the profession. The Virtex-5 LXT design will have an impact on the digital consumer market. The chip will surely find immediate use in the infrastructure products that feed bits to digital devices. Moreover, the lessons Xilinx learned in pushing the process envelope will trickle down into products that directly enable consumer products. Finally, FPGA advancements have time and again scaled over a few short years to meet the cost and power requirements of consumer-design challenges. Well done, Xilinx.

(Now I must get back to work. I think I've already missed my first deadline on the 2007 Innovation Awards planning calendar.) **EDN**

Contact me at mgwright@edn.com.



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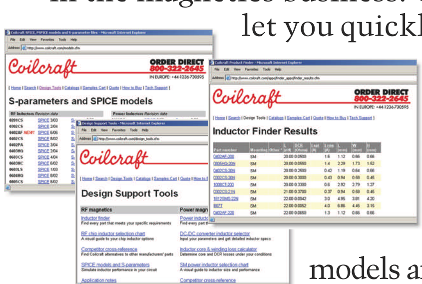

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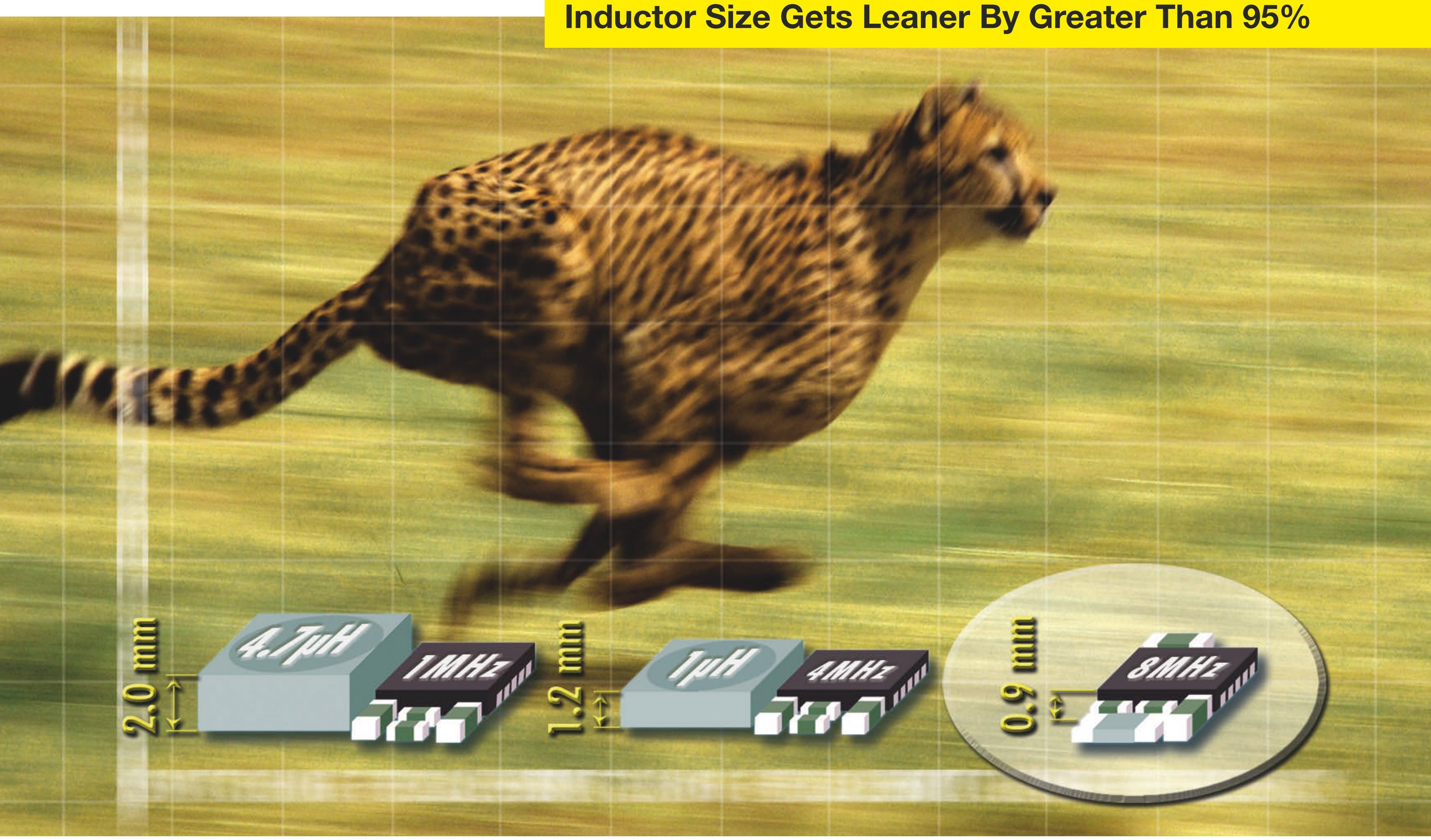

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Generating Precision Clocks for Time-Interleaved ADCs

— *By James Catt, Applications Engineer*

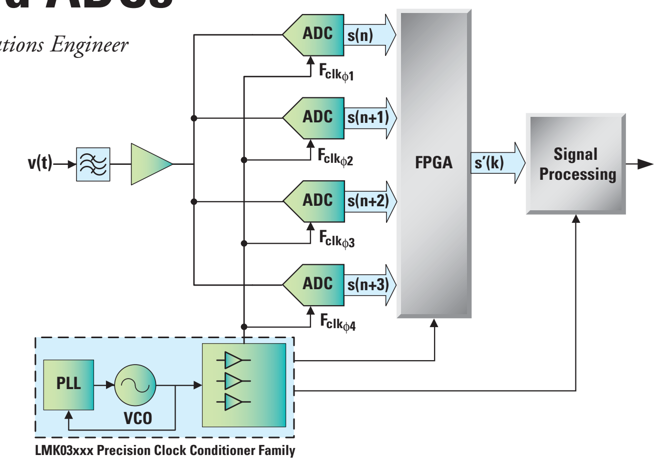

Figure 1. Time-Interleaved ADC System

Many digitized test and measurement applications requiring both high resolution *and* high sampling speeds in excess of what can be delivered by a single Analog-to-Digital Converter (ADC) commonly use multiple ADCs whose sample clocks have staggered phases. Broadband communication systems can also benefit from this architecture. ***Figure 1*** illustrates a *time-interleaved* ADC sampling architecture.

Mathematically, the concept is simple. Even though each ADC is clocked at the same speed, the evenly staggered clock phases result in an effective increase in sample rate. The effective sampling rate is the number of ADCs multiplied by the sample clock. ***Figure 2*** illustrates the time domain relationship between the sample clocks, in this case a four ADC system.

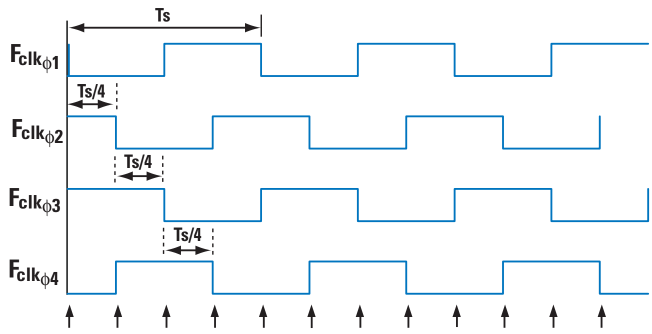

Figure 2. Staggered Sample Clocks For a Time-Interleaved 4-Channel ADC System

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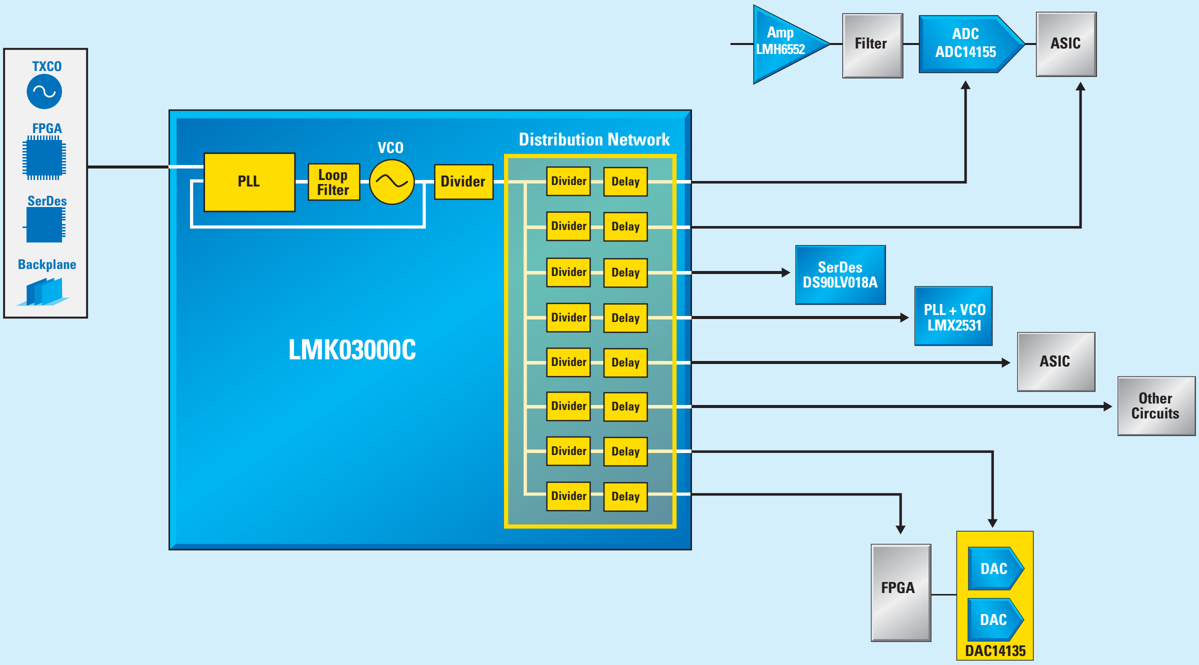

LMK03000/01 and LMK02000 Features

- Fully integrated VCO option delivers unprecedented jitter performance, reducing board space and risk
- Can be configured as jitter cleaner or clock generator
- Available in three performance grades for clocking various high performance applications with diverse jitter requirements
- Footprint compatibility between performance grades
- Three LVDS and five LVPECL clock outputs with dedicated divider and delay blocks simplifies distribution architecture
- Wide clock output frequency range of 1 to 785 MHz
- Small form factor minimizes PCB space by 70%

Performance Grade Table

Performance	Jitter (RMS Typ)
LMK02000	200 fs
LMK03000C/LMK03001C	400 fs
LMK03000/LMK03001	800 fs

Ideal for use in 2G/3G basestations, data converter clocking, networking, medical equipment, instrumentation, military, and aerospace applications

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Generating Precision Clocks for Time-Interleaved ADCs

In *Figure 1* the input to each ADC channel is sampled at the rate of Fs (= 1/Ts) samples per second (SPS). Each ADC sample clock is offset relative to the other sample clocks by a fraction of the clock period Ts. If M is the total number of ADCs, then the fractional phase offset is (in units of one clock period): $\phi_m = \frac{m \cdot T_S}{M}, m = 0,1\ldots,M\text{-}1$

The effective sample rate illustrated in *Figure 2* is $4{\cdot}F_S$. However, the mathematical simplicity belies the complexity of implementing such a system. Hardware imperfections can destroy the performance of the system. In addition to noise and non-linearities that plague all hardware designs, the performance of time-interleaved ADC designs can be degraded by differences in DC offset, gain, and clock skew between the ADCs. *Figure 3* illustrates how these differences are modeled.

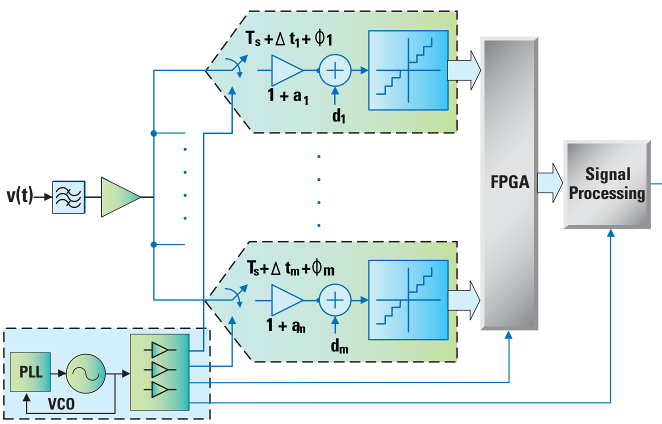

Figure 3. ADC Model with DC, Gain, and Time Skew Offsets

The model in *Figure 3* shows a gain offset parameter a_m for the m-th channel and a DC offset, d_m. The Δt_m parameter applied to the sampling switch instant represents a fixed but arbitrary time skew relative to the ideal sample instant. While the gain and DC offsets are intrinsic to the ADC circuitry, the time skews, Δt_m, originate in the external clocks. The cause of the time-skew may be in the circuit used to create the phase offsets in the clocks, or it may be the result of path length differences in the clock lines. In future articles, these causes will be more fully examined.

All of these imperfections in the ADC channels must be addressed during the system design phase. There is a significant amount of literature that discusses different approaches to compensation and correction schemes for time-interleaved ADC architectures. This article will address the impacts of sample clock time skew and its relation to the topic of precision timing devices.

To gain a better understanding of the impact of the clock skew between ADC channels, a 4-channel time-interleaved system will be analyzed. The time-domain representation of the sampling process is shown in *Figure 4*. The ideal sampling times are indicated by the arrows. The actual sampling times (with skew) are shown as the vertical dotted lines slightly offset from the ideal sampling points. The resulting amplitude errors are replotted on the time axis at the bottom (magnified). In a periodic signal the sampling error due to the clock skew is periodic as well.

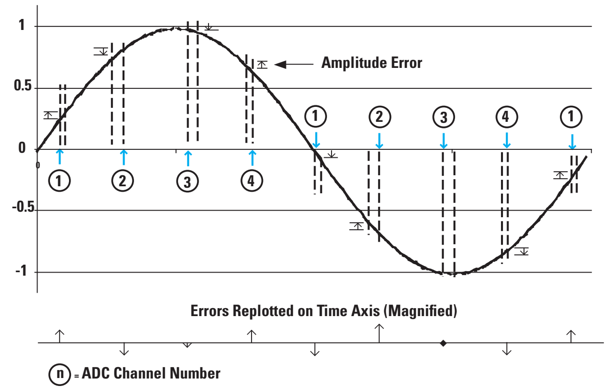

Figure 4. Sample Clock Time Skew Errors in an Time-Interleaved ADC System, M=4

Figure 5 shows another plot of an error signal in a sampled sinusoid due to time skew between clocks. The periodicity of the error signal is clearly seen. Note that the error reaches a maximum at points in the signal where the slope is the steepest.

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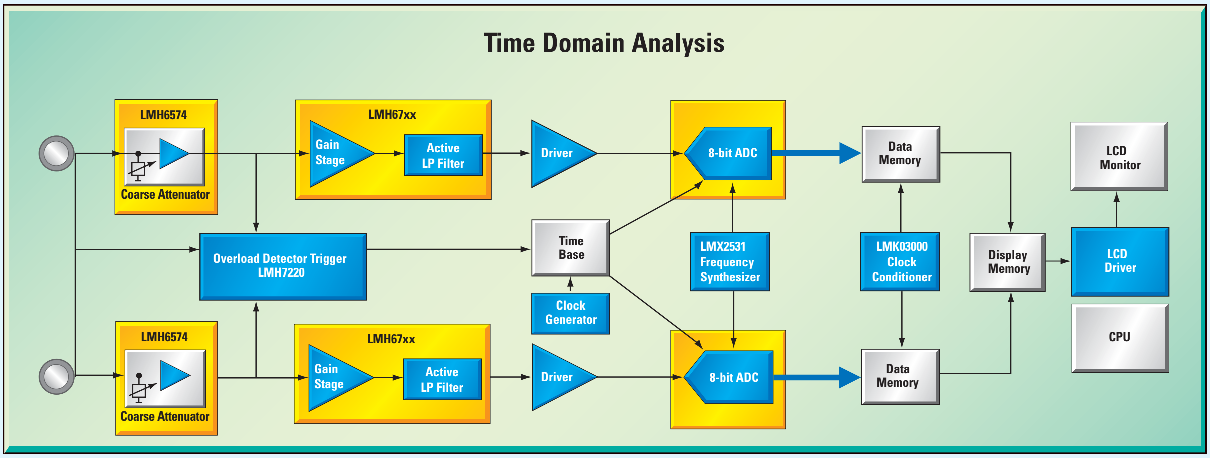

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ADC08D500	8-Bit, dual, 500 MSPS (1 GSPS in DES mode)
ADC08D1000	8-Bit, dual, 1 GSPS (2 GSPS in DES mode)
ADC08D1500	8-Bit, dual, 1.5 GSPS (3 GSPS in DES mode)

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Product ID	Description	Bandwidth/ Propagation Delay	I_{CC} (mA)	Slew Rate (V/µs)	Packaging
LMH6703	High speed, low distortion amplifier	1.2 GHz	11	4500	SOT23-6, SOIC-8
LMH6704	Programmable gain buffer	650 MHz	11.5	3000	SOT23-6, SOIC-8
LMH6574	4-to-1 multiplexer	500 MHz	13	2200	SOIC-14
LMH6550	Differential amplifier	400 MHz	20	3000	SOIC-8
LMH7220	2.9 nsec high-speed comparator with LVDS output	2.9 nsec	6.8	600 psec	TSOT23-6

Clock Conditioners

Product ID	Description	Outputs	VCO	PLL	Jitter (RMS) (typ)
LMK03000C	Clock conditioner	3 x LVDS and 5 x LVPECL outputs	Integrated	Integrated	0.4 ps
LMX2531	Frequency synthesizer	1 x RF output	Integrated	Integrated	0.4 ps

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Generating Precision Clocks for Time-Interleaved ADCs

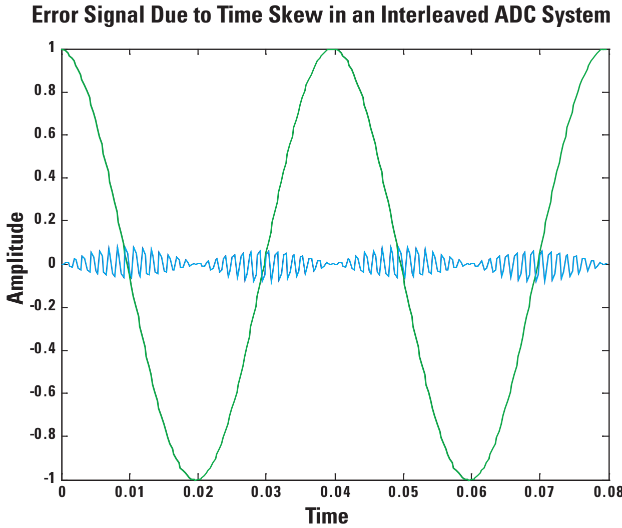

Figure 5. Error Signal Due to Time Skew between Interleaved ADC Clocks, M=4

The frequency domain plot is shown in ***Figure 6.***

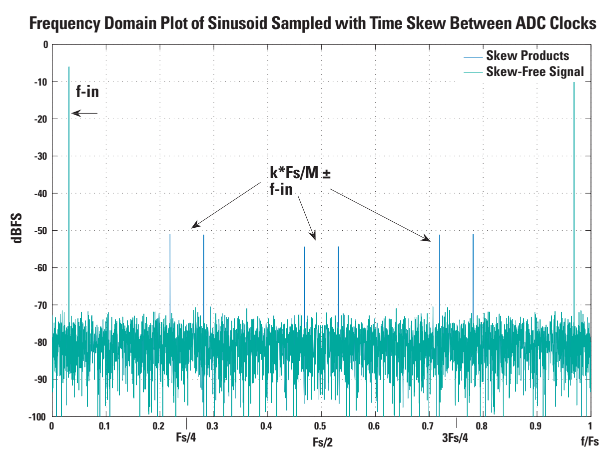

Figure 6. Frequency Domain Plot of Sampled Sinusoid with Spurs Due to Time Skew

If we consider the sample stream $\{s_m(n)\}$ from the ADC in the m-th channel of the system with time skew error, the sample sinusoid can be represented by:

$$s_m(n) = \cos(2\pi f_{IN}(n + r_m)T_s),$$

where r_m = the fixed skew error for the *m-th* ADC channel as a fraction of the sample clock period (T_s), $r_m \in [0,1)$.

Some trigonometric manipulation yields:

$$s_m(n) = \cos\left(\frac{2\pi f_{IN} \cdot n}{f_S}\right) + 2 \cdot \sin\left(\frac{2\pi f_{IN} \cdot r_m}{f_S}\right) \sin\left(\frac{2\pi f_{IN} \cdot (n + \frac{r_m}{2})}{f_S}\right),$$

where fs = sample clock frequency.

The first term in the summation is the desired term, so the 2nd term represents the error due to skew. The amplitude component of this error term depends on f_{IN} and r_m, which should not be a surprise. As f_{IN} increases, the slew rate increases and hence the voltage change over the skew interval increases, leading to increased error. Likewise, as r_m increases, the greater the chance that the signal magnitude will change significantly over the skew interval, also leading to a larger error term. We can see that as r_m goes to zero, the error term goes to zero. There is also an additional frequency component that is in quadrature to the desired component. As indicated in ***Figure 6***, it can be shown that the spurs due to time skew in the multiplexed signal will correspond to $\pm f_{IN} + \frac{k \cdot f_S}{M}$, meaning that they appear as sidebands centered at frequencies $\frac{k \cdot f_S}{M}$, k = 0,1,…,M-1.

In a more noise-like random signal, such as a signal with wideband digital modulation (for example: HDTV, digital cable, WCDMA), the sampling errors due to skew are randomized and so appear as additive random noise and raise the noise floor, decreasing SNR. It should also be clear that increasing skew leads to larger spurs in the periodic signal, and higher noise floor in the modulated signal.

SNR is often the figure of merit that is most indicative of system performance. Hence, the designer needs to be able to predict the degradation in system SNR for some given set of clock skew values. In most cases, however, clock skew can only be controlled to within some interval with some confidence level. In other words, the realized clock skew values and their allocation to different ADC clock inputs are random. Because SNR depends on the random time skew values, it is also a random variable. Therefore, the best we can do is to understand its distribution so that a confidence interval for SNR can be established for a particular distri-

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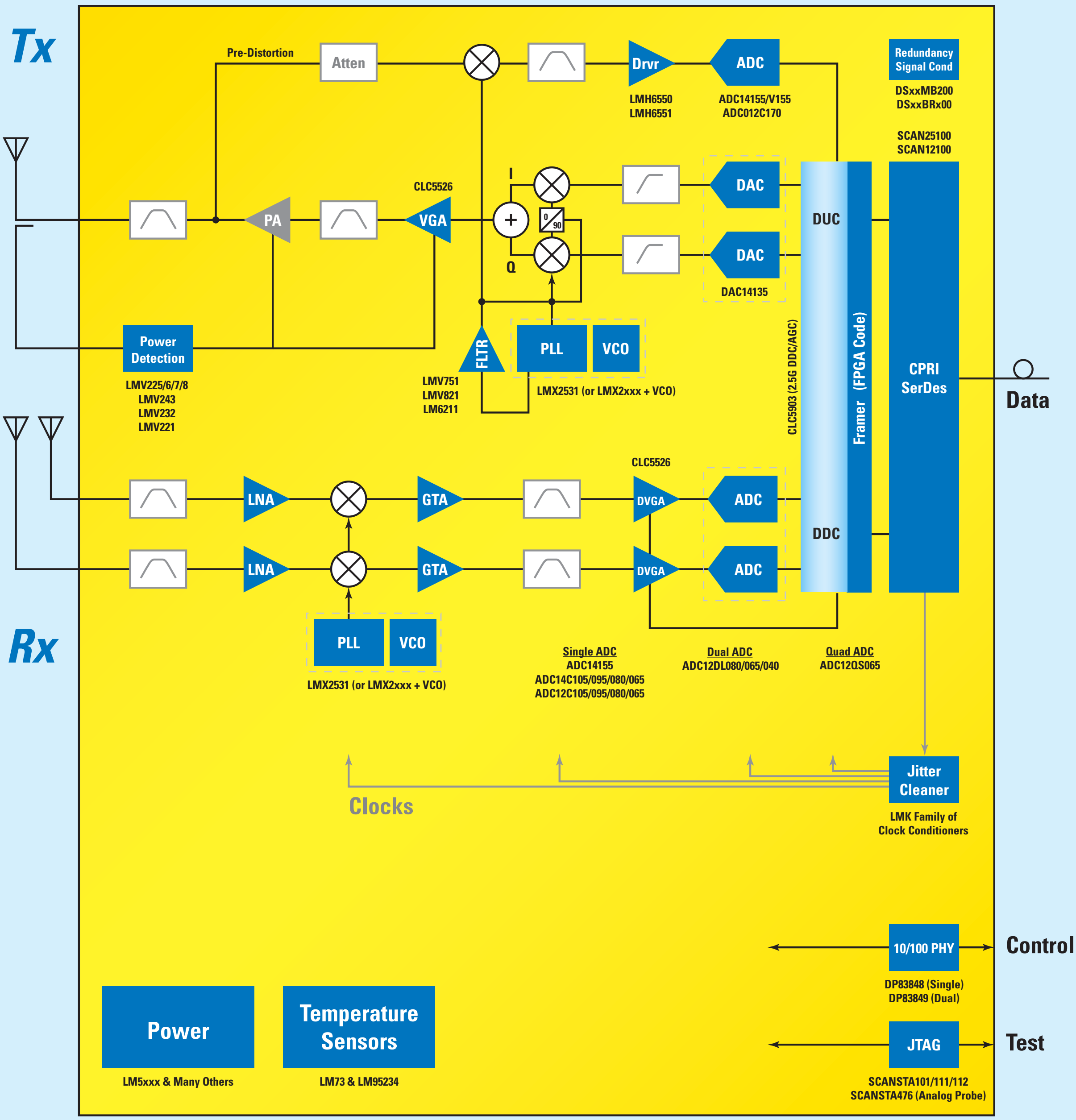

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Generating Precision Clocks for Time-Interleaved ADCs

bution of clock skew values. The key then is relating the statistics of clock skew to the confidence interval for SNR. ***Reference [1]*** addresses this question and derives a closed form of the Probability Density Function (PDF) for SNR that is generalized to any of the ADC channel mismatch parameters. This derivation assumes that the mismatches are Gaussian random variables.

While the closed form expression for the PDF provides good insight, it does not take into account the impact of clock skew in combination with quantization noise. One way to gain insight into these combined effects is to model them using a tool such as Matlab. For example, a 4-channel time-interleaved ADC system model was implemented and simulated in Matlab. The ADCs used in the model employed perfect quantizers so that the distortion contained in the output of the ADC was attributable only to the quantization operation and sample clock skew. Hence, the sensitivity of SNR to clock skew can be isolated from other distortion effects that may also be observed in a sampled signal in the real world. Once a model has been constructed and tested for validity, it can then be used to examine sensitivity relative to the standard deviation of the clock skew and number of time-interleaved ADCs. For example, ***Figure 7*** shows the results of simulations for resolutions of 14 and 12 bits when the input signal is band-limited Additive White Gaussian Noise (AWGN). A Gaussian signal was used in this example because its statistics are similar to many wide-band digital signals. Because skew is a random variable with respect to each ADC clock input, the model allows us to run several thousand simulations in which each simulation run assigns random but fixed values of skew to each ADC clock, drawn from a zero mean Gaussian distribution with a chosen standard deviation (in UI). The SNR is calculated for each simulation run, and a histogram of SNR values is generated after completion of all the runs. Examples are plotted in ***Figure 7***.

The key observation to be drawn from ***Figure 7*** is that for a given Standard Deviation (SD) of the clock skew, in fractions of a unit interval (UI = one clock period), the SNR distribution will be dispersed. A secondary observation is that as expected,

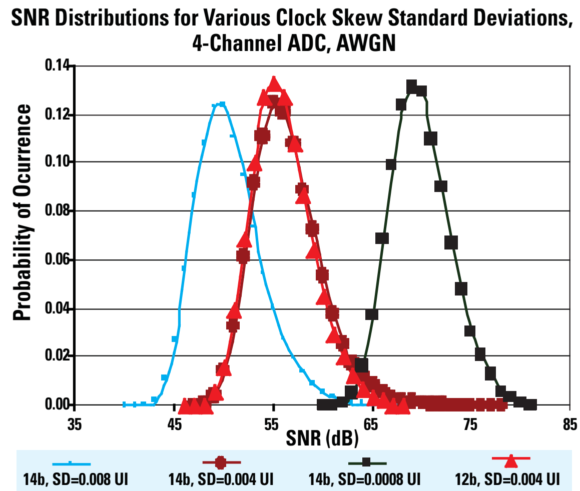

Figure 7. SNR Distributions for a 4-Channel Interleaved ADC System with Various Skew Distributions

SNR degrades as the standard deviation of the clock skew increases. In the 14-bit case, we see that when clock skew reaches 0.8% UI, the SNR of the sample stream has seriously degraded. Because most designs must meet a minimum target SNR, the histogram data represented in the plots in ***Figure 7*** enable the designer to begin evaluating design specifications for the clocking system driving the time-interleaved ADCs. The 90%, 95%, and 99% confidence intervals for SNR associated with a particular clock skew distribution can be estimated from the histogram data, allowing the designer to determine the suitability of a clocking design exhibiting such performance.

Summary

In this article, we have examined the impact of sample clock skew on time-interleaved ADC systems. National's LMK03xxx family of Precision Clock Conditioners with integrated VCO features multiple clock outputs that are locked to a single reference. These outputs may be edge synchronized, or, alternatively, programmable delay may be assigned to each clock output. Because path length differences can impact skew between clocks, having an adjustable delay capability is an important tool when designing a clocking scheme for a time-interleaved ADC system.

[1] G. Leger, E. J. Peralias, A. Rueda, J. L. Huertas, "Impact of Random Channel Mismatch on the SNR and SFDR of Time-Interleaved ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers,* Vol. 51, No. 1, January 2004.

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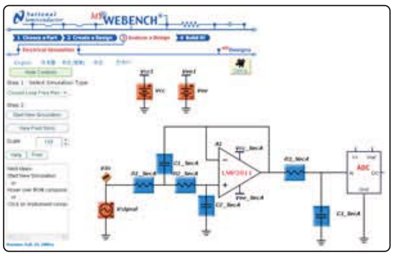

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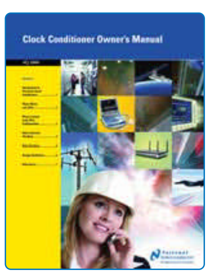

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INNOVATIONS & INNOVATORS

Module mixes GPS, cellular functions

Transportable embedded systems, such as those in the railway industry, must be able to pinpoint their location and communicate from diverse locations, including areas with very low signal strengths. MEN Micro Inc targets these applications with its new, 3U, single-slot CompactPCI interface card with a 12-channel, parallel GPS (global-positioning-system) receiver for location data and a GSM (Global System for Mobile communication) device for cellular communications. The new F210 GPS/GSM/UART-interface card supports the GSM 850, EGSM 900, GSM 1800 and GSM 1900 frequency bands, as well as the NMEA (National Marine Electronics Association) 0183 protocol.

The F210 CompactPCI interface card delivers location information and reliable wireless communications in low-signal-strength areas.

The 32-bit, 33-MHz F210 incorporates two SA-Adapter slots for serial interfaces with RS-232, RS-422, or RS-485 line drivers, either with or without optical isolation. SA-Adapters are small universal boards allowing designers to mix and match legacy serial I/O, fieldbus interfaces, and other small I/O functions. Reverse SMA connectors provide the physical interface to the external GPS and GSM antennas. The board features an extended temperature range of −40 to +85°C and will be available in June 2007. The price of the F210 is $1719.**—by Warren Webb**

▷**MEN Micro Inc**, www.menmicro.com.

FEEDBACK LOOP

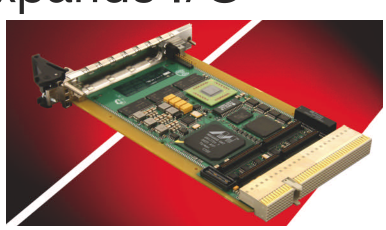
"I see IP (intellectual property) as morphing from a knowledge-intensive to a service-intensive industry. The biz model will have good quality taken as default and the service as the differentiating and, thus, cost-driven factor. Of course, given an average customer's psyche, if he is asked to pay for something that he considers should be present by default—in this case, quality—he'll say, 'no!'"

—Meenu, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6412357. Add your comments.

Board computer expands I/O

As the 3U CompactPCI form factor gains popularity for space-constrained, high-performance applications, designers are looking for off-the-shelf components that they can adapt to a range of system configurations. The new SCP/DCP-124P single-board computer from Curtiss-Wright Controls Embedded Computing provides this flexibility by directly mapping the onboard PMC-module I/O pins to the backplane. The company designed the device for use in CompactPCI-backplane-peripheral slots, and it can satisfy multiple I/O functions depending on the installed PMC module.

Available in both conduction- and air-cooled versions, the SCP/DCP-124P supports a full 64-bit, 100-MHz PCI-X-capable PMC site along with additional built-in I/O. Providing power to the board, Freescale's (www.freescale.com) Altivec-enhanced 7448 PowerPC processor includes 1 Mbyte of internal cache memory and as much as 1 Gbyte of DDR SDRAM with ECC (error-correcting code). The SCP/DCP-124P's PCI bus operates at 33 or 66 MHz and supports both 3.3 and 5V signaling. The module also optionally includes two 10/100/1000BaseT Ethernet ports, two serial channels, 12-bits of TTL discrete I/O, and two USB 2.0 ports. Software support includes board-support packages for VxWorks, Tornado, Workbench for PowerPC, CWCEC (Curtiss-Wright Controls Embedded Computing) Linux, and Integrity. Prices for the SCP/DCP-124P start at $6030.

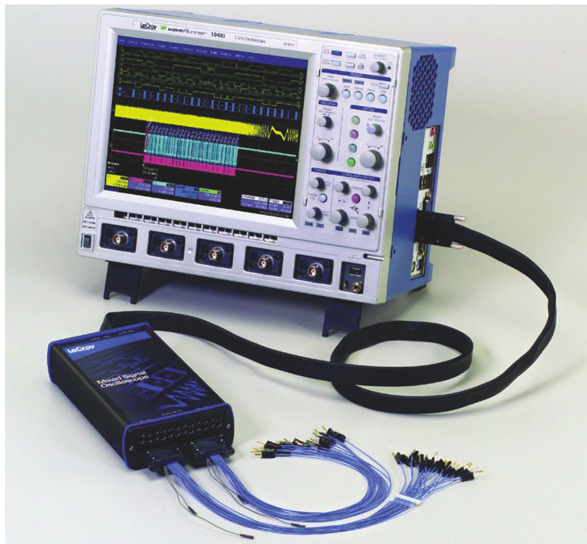


The SCP/DCP-124P CompactPCI single-board computer supports PMC I/O through the backplane.

—by Warren Webb

▷**Curtiss-Wright Controls Embedded Computing**, www.cwcembedded.com.

MSOs: Tektronix re-enters the field; deeper memory becomes de rigueur



Most of the electronics associated with the logic-analysis capabilities of LeCroy's large-screen, slim-footprint WaveSurfer and WaveRunner MSOs reside in the logic pod (foreground).

If Tektronix wanted to, it could make the case that it was the first major oscilloscope manufacturer to offer an MSO (mixed-signal oscilloscope). More than a decade ago, Tek offered an instrument, the TLS216, that you might call the forerunner of today's MSOs. Nevertheless, credit for popularizing the MSO usually goes to Agilent, whose large array of moderately priced, capable, easy-to-use products has attracted a broad following—especially among embedded-system developers. The size and breadth of that following didn't escape the notice of Yokogawa and LeCroy, both of which have, within the past couple of years, added MSOs to the popularly priced families in their digital-scope-product lines.

Meanwhile, Tek, which had long ago discontinued the TLS216, maintained that a scope and a full-featured logic analyzer operating in concert with Tek's iView software could perform many important debugging tasks that MSOs can't handle—for example, disassembly of microcontroller instructions captured from a bus, thus enabling users to trace program flow. Still, Tek could not deny the utility of the popularly priced oscilloscope-based instruments, which, in one chassis, combine 16 or more channels of logic-timing analysis and as many as four analog channels.

However, with one firmly entrenched competitor and two more that also provide versatile, high-quality products, Tek's new entry into the MSO market had to offer exceptional value and capabilities. Its new MSO4000 series, with prices starting at $8700, meets those requirements and offers, among other features, 10M-sample/channel digital-memory depth on 16 logic channels.

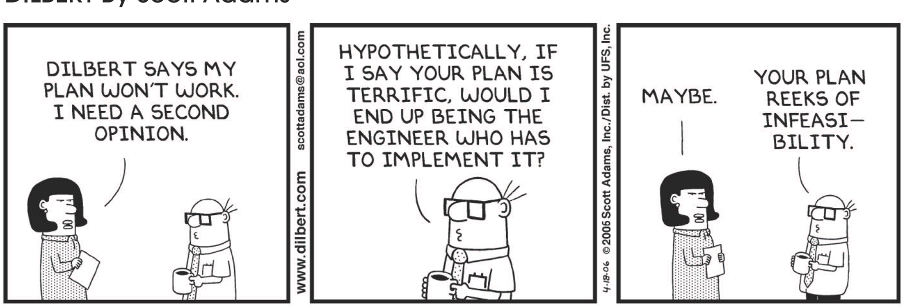
A day before Tek announced its units, LeCroy announced new MSOs in its WaveRunner Xi and WaveSurfer Xs families. These units, with prices starting at $9180, offer digital-memory depth as great as 50M points/channel and can acquire and display data from 18 or 36 digital inputs. Full-featured logic analyzers from Agilent and Tek provide modularity in groups of 34 channels because data-bus widths are multiples of eight channels, and users need additional channels to observe clocks and other synchronization signals. Nevertheless, among the four major suppliers, only LeCroy's MSOs currently offer 18/36-channel modularity. Yokogawa's new, $23,495 DL9710L offers 32 digital channels. Most other MSOs provide 16 digital channels.

Part of the reason that LeCroy and Yokogawa can offer more channels is their architectural approach; the digital-acquisition capability resides not within the instrument mainframe, but in a small, external, multichannel-logic pod. Although it plugs into the rear of the instrument through a flexible cable (flat in LeCroy's case, round in Yokogawa's), the pod is small enough that you can easily place it near the unit under test. Attaching probes to such a pod is more convenient than attaching them to the instrument's rear panel—which was necessary on some older MSOs.

The manufacturers clearly believe that the physical attributes of an MSO are of great importance to potential buyers. In particular, LeCroy and Tektronix have packaged their new products in shallow cases, which provide 10.4-in. screens and occupy a minimum of benchtop area. With so many traces on display, the large screens—and the ability to attach even larger external monitors—are important, but so is the need for the test setup to stay within the confines of the benchtop.

With a few exceptions, MSOs neither capture analog and digital signals at the same sampling rates nor offer equal analog- and digital-record lengths (as measured in record duration or in num-

DILBERT By Scott Adams



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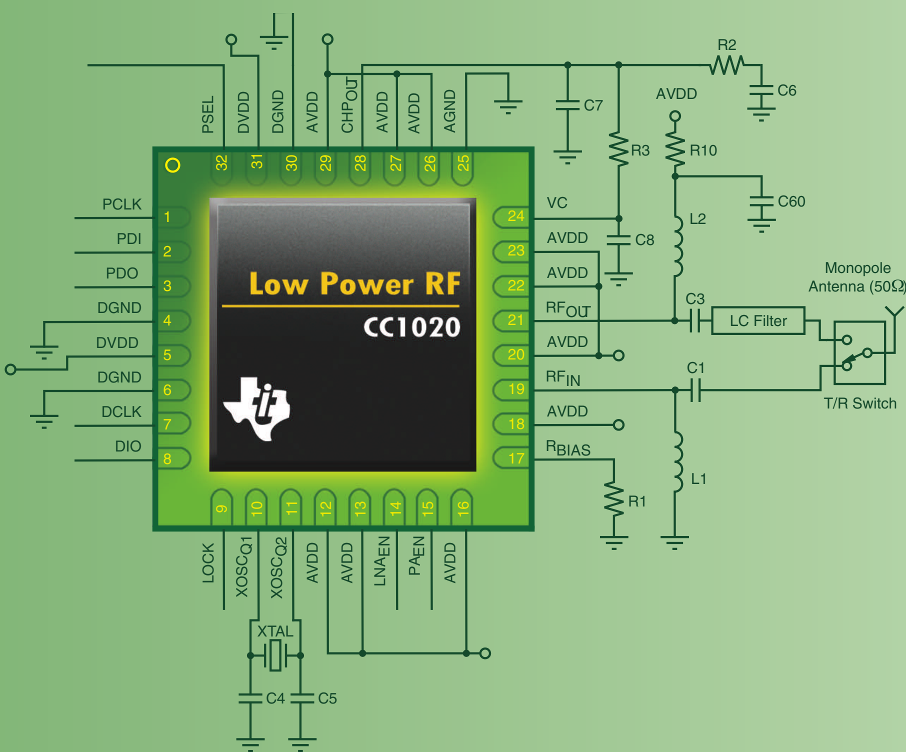

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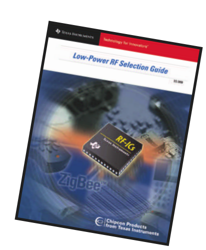

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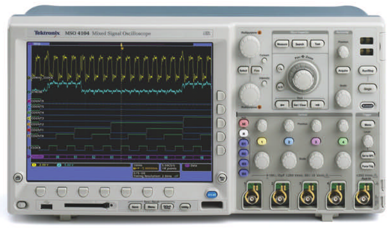
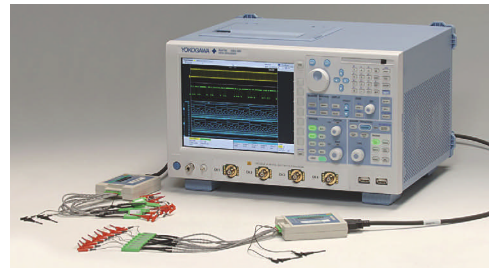


Tektronix's MSO4000-series units bring to the MSO world several innovative features, including ultrahigh MagniVu sampling rates and the ingenious use of color to enhance ease of use.



Like LeCroy, Yokogawa, in its DL9710L MSO, places most of the electronics associated with acquiring digital signals in the small pods into which you plug the digital probes.

ber of acquired data points in the record). The instruments do, however, trigger acquisitions on all channels based on combinations of digital and analog events and accurately time-align the analog and digital waveforms they display.

Tek's MSO4000 units also incorporate the MagniVu feature you find in many of the company's full-featured logic analyzers. This capability enables each logic channel to acquire 10,000 samples (5000 before the trigger point and 5000 after) at real-time rates as great as 16.5G samples/sec, or one sample on each channel every 60.6 psec. This speed is more than twice that of the MagniVu mode of the company's full-featured logic analyzers, which can capture one sample per channel every 125 psec.

In conjunction with the high capture rate, the MSO4000 units use color to draw attention to easily overlooked phenomena that often divulge their secrets when you examine the details with MagniVu. If it determines that multiple logic-state transitions of one to zero or zero to one have occurred in regions of the screen too narrow to expose their full content, the instrument displays in white what appear to be edges or pulses. When you scroll through the display, these areas stand out. Sometimes, simply magnifying the timebase uncovers the details. If not, triggering on the suspect points and expanding them with MagniVu can reveal the unit under test's true behavior. Another innovation uses different colors to display signals in the logical-one and -zero states, eliminating the need to scroll back and forth to determine the state of signals that remain constant across more than one full screen width.

Many more features are unique to individual manufacturers. Agilent, for instance, boasts of its frame rate of more than 100,000 waveforms/sec, a consequence of the company's proprietary MegaZoom architecture. As appropriate for instruments that target embedded-system developers, all of the MSO manufacturers offer support for popular buses, such as I^{2}C (inter-IC), CAN (controller-area network), SPI (serial-peripheral interface), and RS-232. The support packages' features, of course, differ.

The **table** compares the features and prices of four MSOs, one from each of the major manufacturers. The shallowest base digital-memory depth in any of these products is 2M samples/channel; an option increases the 2M figure to 8M samples/channel. A depth of 10M samples/channel appears popular, and one supplier offers configurations that can capture 50M samples/channel. At 500M samples/sec, a 10M-point record represents only 20 msec—one acline cycle in much of the world. Without question, though, the manufacturers also believe that MSOs lacking in deep memory are *so* last year.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com.
▷**LeCroy Corp**, www.lecroy.com.
▷**Tektronix Inc**, www.tektronix.com.
▷**Yokogawa Corp of America**, www.yokogawa.com/us.

REPRESENTATIVE MIXED-SIGNAL OSCILLOSCOPES FROM FOUR LEADING MANUFACTURERS[1]

Manufacturer	Model	Base US list price	No. of analog channels	Analog bandwidth (GHz)	Maximum analog sampling rate (samples/sec)[2]	Base analog memory depth (samples per channel)[2]	Maximum analog memory depth (samples per channel)[3]	Maximum digital channels	Maximum logic-toggle rate	Base digital-memory depth (samples per channel)[3]	Maximum digital-memory depth (samples per channel)[3]
Agilent	MSO6104A	$16,535	Four	1	4G	2M	8M	16	250 MHz	2M	8M
LeCroy	WaveSurfer 24Xs	$9180	Four	0.2	2.5G	2.5M	10M	36	500 MHz	10M	50M
Tektronix	MSO4032	$8700	Two	0.35	2.5G	10M	10M	16	8 GHz[4]	10M	10M
Yokogawa	DL9710L	$23,495	Four	1	5G	6.25M	6.25M	32	250 MHz	6.25M	6.25M

Notes:
[1]The entries do not show the manufacturers' full MSO-product lines. For additional information, consult the manufacturers' Web sites.
[2]Some units can achieve the maximum analog sampling rate and stated analog-memory depth only when you use no more than half of the analog channels.
[3]Some units achieve the stated maximum digital-memory depth only when you switch off the associated analog channel.
[4]In normal mode, the maximum sampling rate is 500 MHz, resulting in an ability to display a toggle rate of almost 250 MHz. MagniVu mode allows viewing logic waveforms that toggle at approximately 8 GHz.

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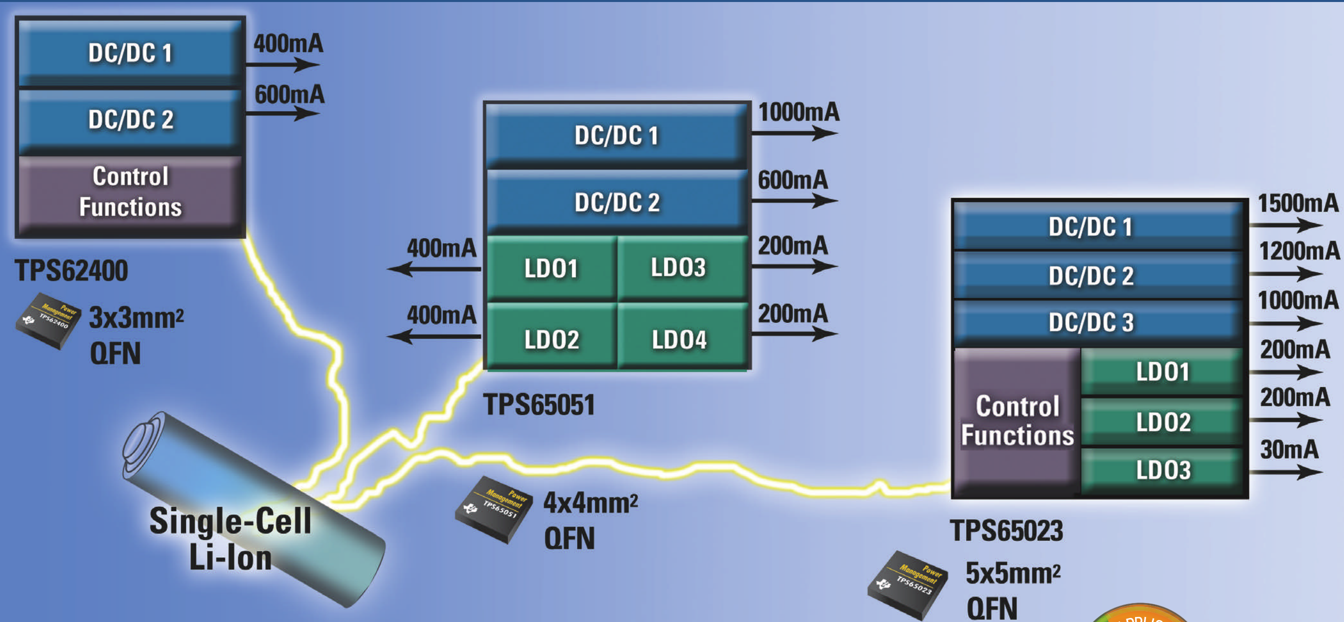

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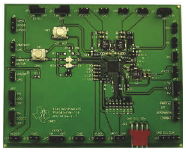
TPS62400	2	–	2	2.25MHz	0	EasyScale™	2.5 to 6.0	3x3mm^2	General Purpose	$2.50
TPS65010	4	Yes	2	1.25MHz	2	I^{2}C	2.5 to 20	7x7mm^2	TI OMAP™ Platform	$3.30
TPS65020	6	–	3	1.5MHz	3	I^{2}C	2.5 to 6.0	6x6mm^2	TI DM320, Marvell PXA270	$3.75
TPS65023	6	–	3	1.5MHz	3	I^{2}C	2.5 to 6.0	5x5mm^2	TI DaVinci™ Technology	$3.85
TPS65050	6	–	2	2.25MHz	4	–	2.5 to 6.0	4x4mm^2	Samsung S3C241x	$2.75
TPS65051	6	–	2	2.25MHz	4	–	2.5 to 6.0	4x4mm^2	TI OMAP850, Marvell PXA255	$2.75
TPS65820	12	Yes	3	1.5MHz	7	I^{2}C	3.0 to 18	7x7mm^2	General Purpose	$6.50

** Suggested resale price in U.S. dollars in quantities of 1,000.*



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APEC highlights what's hot in power

A strong electronics market coupled with the public's recognition that power efficiency is in everyone's best interest resulted in high traffic at the power-conversion industry's annual APEC (Applied Power Electronics Conference) 2007, which took place in February in Anaheim, CA. The power technologies that are currently hot topics are discrete semiconductors—a no-brainer, given that APEC is the show at which MOSFETs shine; POE (power over Ethernet); and power-control and -management ICs.

Switching FETs: Vendors Fairchild Semiconductor, Toshiba, Infineon (www.fairchildsemi.com, www.toshiba.com, www.infineon.com), and others displayed products employing this technology. Fairchild bundled the driver with the FET switch in the FDMF8700 multichip module for use in buck converters with currents as high as 30A at 1 to 1.2V. The devices support Intel's (www.intel.com) DrMOS V_{CORE} dc/dc-converter standard. Toshiba made a family of high-speed switching MOSFETs available for sampling. The family uses the company's UMOS-V, a fifth-generation ultrahigh-speed process technology that improves power efficiency. The 11 initial members of the family are 30V, N-channel single MOSFETs with low on-resistance. Meanwhile, Infineon demonstrated both its 30V OptiMOS 3 power semiconductors and CoolMOS CP series, which it introduced at the end of last year. Vishay (www.vishay.com) introduced its SkyFET technology, which integrates a Schottky diode into a FET, increasing switching speed and lowering the parasitics associated with using an external diode. Vishay also introduced three OR-ing MOSFETs for redundant applications.

POE: Power Integrations (www.powerint.com) introduced the DPA422-426 dc/dc-converter IC for 10W POE applications. According to Andy Smith, product-marketing manager for the company's DPA-switch family, look for an update to the POE standard in the second half of the year. The update will boost the allowable device power from 10 to 30W and, he predicted, result in a surge in POE-device sales. In addition, Freescale (www.freescale.com) and Texas Instruments (www.ti.com) demonstrated POE chips that they introduced in the fourth quarter of 2006.

Power-control and -management ICs: Micrel (www.micrel.com) joined Power-One's (www.power-one.com) Z-Alliance (www.z-alliance.org) of power-supply and semiconductor manufacturers offering products and components for the Z-One digital-power architecture. Micrel's MIC68400 family of low-dropout regulators targets FPGAs, DSPs, and microcontrollers that require a controlled start-up. The advantage of a control protocol, such as Z-One, is that it requires no intelligence in the regulator; in its simplest form, it's just an enable pin. Intersil (www.intersil.com) introduced the PMBus (www.pmbus.org)-compliant ISL8601 PWM controller with integrated MOSFET drivers. Technical Marketing Manager Zaid Salman, an advocate of the PMBus, pointed to the fact that Intel recently adopted it as further validation of the open standard. The chip supports power-up and -down protocols, such as sequencing, tracking, and ratiometric tracking; you hardware-select the protocol through external passive components. You can also daisy-chain the chips to sequentially power up or power down.

—by Margery Conner

▷**Applied Power Electronics Conference**, www.apec-conf.org.

XILINX GOES NONVOLATILE WITH SPARTAN-3AN FPGA

Xilinx is jumping into the nonvolatile-FPGA market with the Spartan-3AN device. The SIP (system-in-package) device incorporates a 90-nm, SRAM-based Spartan-3A FPGA die atop a NOR-flash die. The Spartan-3A communicates with the NOR through four pins in the middle of the Spartan-3A.

SRAM-based FPGAs typically boast better performance and greater capacity than their nonvolatile counterparts, but SRAM-based FPGAs lag behind nonvolatile FPGAs in stability and security. Nonvolatile devices retain their data and programming when users turn off the power. SRAM devices, on the other hand, lose their data when the power is off and, when on, must access an outside memory to configure the FPGA. During this step, clever thieves could tap into the memory-to-FPGA interconnect and steal the design. Nonvolatile FPGAs also seem more secure, as FPGA vendors and their customers move into areas lacking well-established IP (intellectual-property) laws or to applications placing a high priority on data retention.

That security has been the marketing cry and the selling point for Actel (www.actel.com), which has for several years offered nonvolatile FPGAs. With the release of Spartan-3AN, Xilinx seems to concur with that message.

Xilinx Chief Executive Officer Wim Rholandts told reporters at the GlobalPress 2007 Summit that the new Spartan-3AN, like the Spartan-3A, will go after the triple-play market of voice, video, and data.

The 3AN includes the features of the 3A, such as two low-power hibernate modes and what Xilinx calls Device DNA to further protect the device from cloning and overbuilding. But the additional NOR flash boosts the embedded memory to 16 Mbytes, which allows the device to hold two SRAM configurations. The two-die configuration boasts 100,000 write/erase cycles, write and erase protection, and advanced memory partitioning.

Xilinx will offer five versions of the Spartan-3AN, ranging from 50,000 to 1.4 million system gates with as much as 576 kbytes of block RAM, 16 Mbytes of embedded flash, and as many as 502 I/Os supporting 26 I/O-protocol standards. The company is shipping the XC3S200AN, XC3S700AN, and XC3S1400AN devices, and all five devices will be in production by the third quarter of this year. Xilinx's ISE 9.1i design-tool suite and Spartan-3 Generation library of application-specific IP support the product.–by Michael Santarini

▶ **Xilinx Inc, www.xilinx.com.**

VOICES

Analyst Gary Smith: Semiconductors need a parallel-processing language

For nearly two decades, analyst Gary Smith has been a fixture in the EDA industry—advocating new tool flows and methodologies as the silicon times have changed. Late last year, Gartner Dataquest closed Smith's EDA-analyst group, but the former LSI Logic IC-design-flow methodologist and 25-year semiconductor veteran has started his own analyst company, GarySmithEDA (www.garysmitheda.com). *EDN* recently asked his opinions on the state of the design business.

What has been the biggest change in the chip business since you started as an analyst?

A The biggest change has been the move from component suppliers to system-IC vendors. That change is affecting all of the electronics market. Basically, ICs were always components. You put them together on a PCB [printed-circuit-board] to make systems. But, as we got more and more gates available to us, what we saw was a group of semiconductor vendors that moved out of the component-based market into the subsystem or even system market. They were actually doing the systems design.

You mean rather than doing a system on a board, they were doing an SOC (system on chip)?

A Yeah, and because it was now on-chip, the semiconductor guys were doing it, not the OEMs. Probably the best example is TI's OMAP [Open Multimedia Applications Platform] for the handheld market. Suddenly, we see the IC vendors determining system architectures. It's been a big, important shift. We still have a lot of component vendors, but the leading guys are system-IC vendors.

What are the hot IC-design-related topics this year?

A Software, software, software, and then DFM [design for manufacturing] and the move to an ESL [electronic-system-level]-driven verification methodology. But software's the biggest problem, and it needs to be solved. If anything slows down the industry, it is going to be a lack of embedded-software infrastructure for parallel processing. To solve the power problem, which started a few years ago, we started going to slower designs with multiple processors onboard. And, as we started getting more gates to work with, we started adding more processors to products like cell-phone designs. We're walking away from von Neumann architecture. Unfortunately, the software architecture is based on the von Neumann community's using C

as a language, and it is all sequential. We've been trying to solve the parallel-[computing] problem since 1985, but the semiconductor vendors are at a point where they say "we've got to do it." Semiconductor vendors want to keep adding more processor cores—moving from four to eight to 16 to 1000—to their silicon, but the software guys are saying "I don't know why we can't program it." We are reaching this cliff that, if we don't solve the problem, the semiconductor industry is in trouble.

I saw this neat design the other day; it had 175 processors. One was working its ass off, and the other 174 were keeping it warm. DARPA [Defense Advanced Research Products Agency, www.darpa.mil] recently funded Sun Microsystems, AMD, and Cray [www.sun.com, www.amd.com, www.cray.com] to come up with a concurrent-design language, and there is serious work going on at IBM, Intel, and ARM. The ITRS [International Technology Roadmap for Semiconductor, www.itrs.net] is also on the case, so now folks are starting to realize this is a big deal.

The 130- and the 90-nm nodes both required retoolings. When do you think the next retooling will occur?

A It happens every two nodes. We are now beginning the move from 65- and 45-nm tools to 32- and 22-nm tools. The 65-nm node wasn't nearly as hard as we expected. Typically, the first of the two processes [when there's been a significant change in IC manufacturing, such as the introduction of copper at 130 nm] is the most difficult, and that's when the power users [designers of the most advanced chips] need new tools. Unfortunately, it usually takes the EDA industry a bit of time to catch up and offer tools for new problems.

Will high-k dielectric have a big impact and force a retooling?

A It will have an impact. They are now talking about new materials and a two-mask process; there are going to be a lot of changes that may cause ripples in the design flow. We are starting to do 45-nm designs now. We should have had 45-nm tools in September, but we don't seem to have them yet.

What tools or skills will the retooling require?

A On the silicon end, it requires model-based DFM; on the complexity side, it requires a solid ESL flow.

Who are the up-and-comers in the EDA business? Are there any hot start-ups on the horizon?

A In DFM, keep an eye on Clear Shape [www.clearshape.com] and Blaze DFM [www.blaze-dfm.com]. In ESL, keep your eye on CoWare, Mentor, and The Mathworks [www.coware.com, www.mentor.com, www.mathworks.com]. For the start-ups, Imperas [www.imperas.com] stands out. It is one of the companies that is trying to come up with a language for parallel processing. There are a few others, but I still haven't met with them yet to see what they are really doing.

—by Michael Santarini

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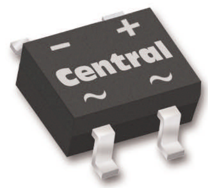

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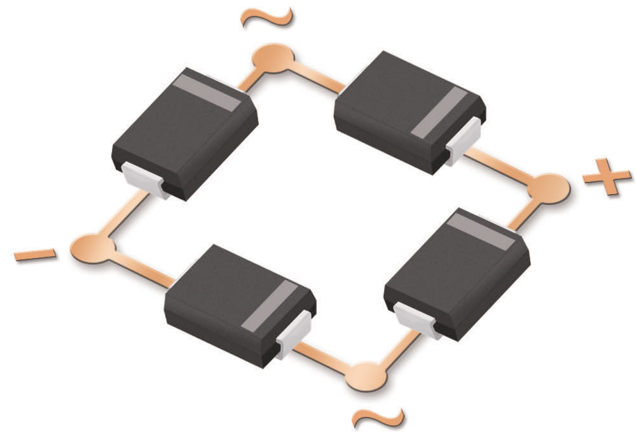

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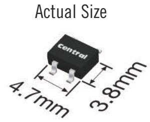

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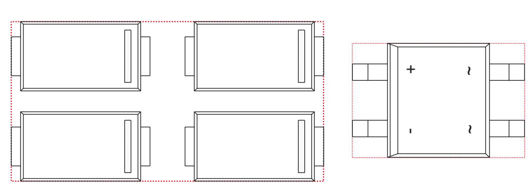

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BY BONNIE BAKER

Wringing out thermistor nonlinearities

Thermistor-temperature-sensing devices present a design challenge if you intend to use such a device over its entire temperature range. Typically, the thermistor is a high-impedance, resistive device that eases one of the interface issues as you convert the thermistor resistance to voltage. The more difficult interface challenge is to capture the nonlinear behavior of the thermistor in a digital representation with a linear ADC.

The term "thermistor" originates from the descriptor "thermally sensitive resistor." The two basic types of thermistors are negative- and positive-temperature-coefficient devices. The negative-temperature-coefficient thermistor best suits precision temperature measurements. You can determine the surrounding thermistor temperature by using the Steinhart-Hart equation: $T=1/(A_0+A_1(\ln R_T)+A_3(\ln R_T^3))$. In this equation, T is the temperature in degrees Kelvin; R_T is the thermistor resistance at temperature T; and A_0, A_1, and A_3 are constants that the thermistor manufacturer provides.

The thermistor-resistance change over temperature is nonlinear, as the Steinhart-Hart equation describes. When measuring temperature, drive a reference current through the thermistor to create an equivalent voltage. This equivalent voltage has a nonlinear response. You can try to compensate for the thermistor's nonlinear response with a look-up table in your microcontroller. Even though you can run this type of algorithm in your microcontroller firmware, you need a high-resolution converter to capture data during temperature extremes.

Alternatively, you can use hardware-linearization techniques before digitization and a lower resolution ADC. One technique is to place a resistor, R_{SER}, in series with the thermistor, R_{THERM}, and a voltage reference or the power supply (**Figure 1**). Setting the PGA (programmable-gain amplifier) at a gain of 1V/V, a 10-bit ADC in this circuit can sense a limited temperature range (approximately ±25°C).

In **Figure 1,** note that resolution is lost at high temperatures. Increasing the PGA's gain at these temperatures brings the output signal of the PGA back into a range at which the ADC can reliably provide conversions that identify the thermistor temperature.

The microcontroller firmware's temperature-sensing algorithm reads the 10-bit-ADC digital value and passes it to a PGA hysteresis-software routine. The PGA hysteresis routine checks the PGA gain setting and compares the ADC digital value with the trip points that **Figure 1** indicates. If the ADC output is beyond a trip-point value, the microcontroller sets the PGA gain to the next higher or lower gain setting. If necessary, the microcontroller can again acquire a new ADC value. The PGA gain and ADC value then pass to a microcontroller piecewise linear-interpolation routine.

Obtaining data from a nonlinear thermistor sometimes can seem like an impossible task. You can combine a series resistor, a microcontroller, a 10-bit ADC, and a PGA to overcome the measurement difficulties of a nonlinear thermistor across a temperature range greater than ±25°C. EDN

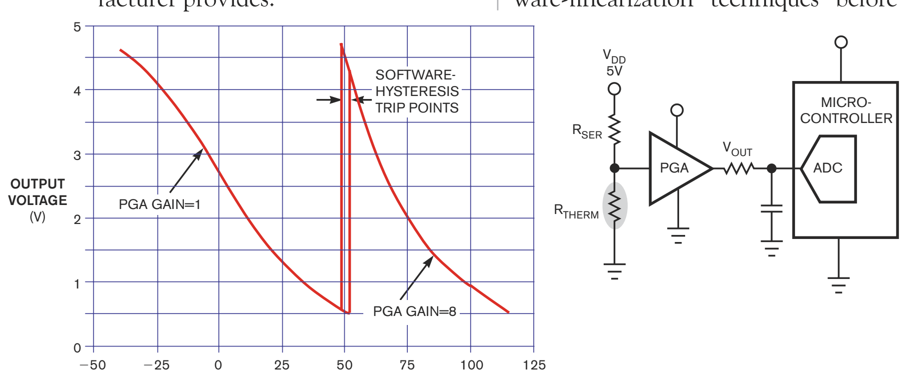

Figure 1 You can tame the nonlinear response of the thermistor, R_{THERM}, with a series resistor, R_{SER}; a PGA; and a microcontroller.

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2 "Introduction to NTCs: NTC Thermistors," BC Components data sheet, March 27, 2001, www.vishay.com/company/brands/bccomponents/.

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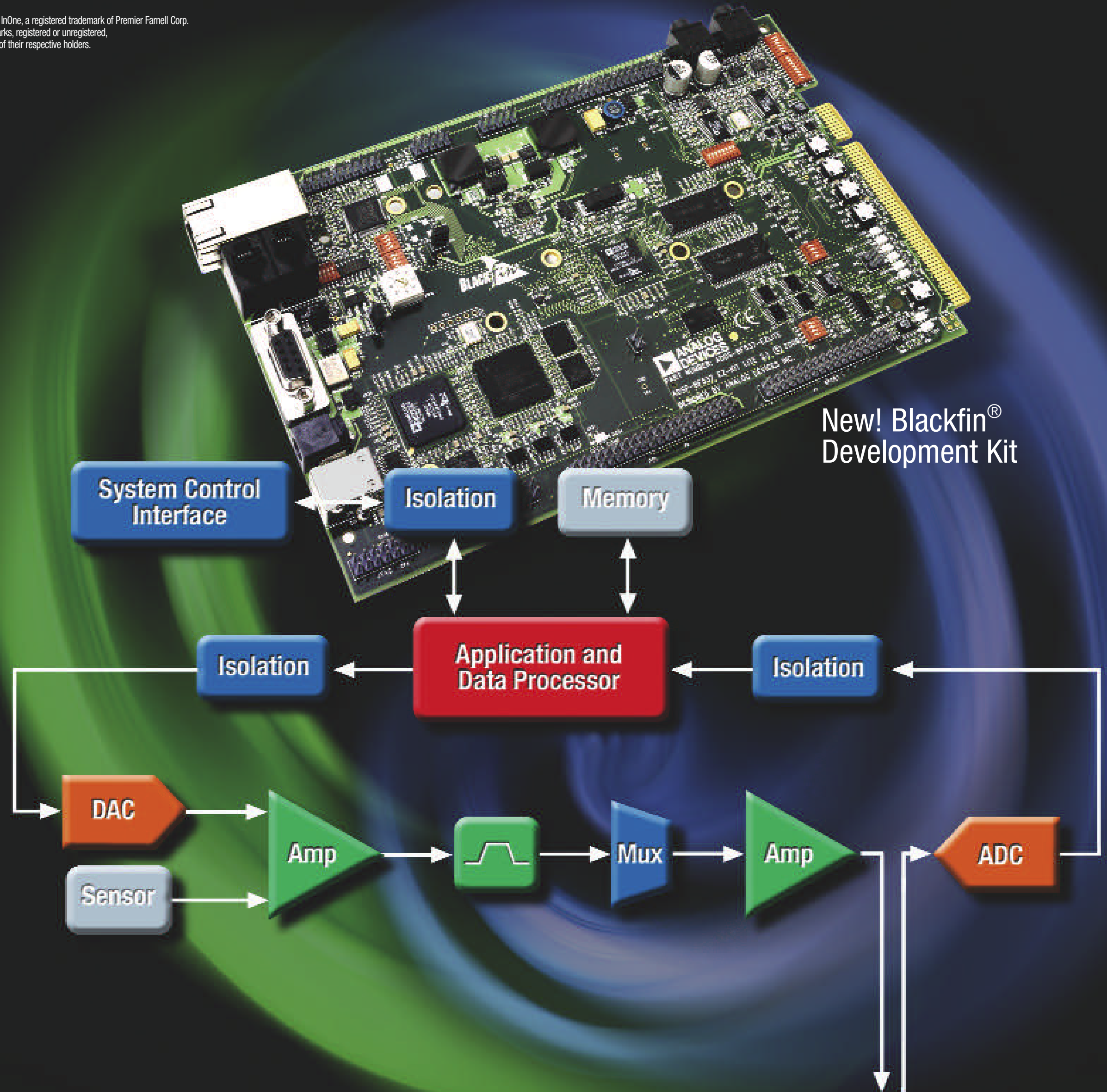
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Fooled by a thermocouple

DANIEL VASCONCELLOS

During the development of a medical product requiring noninvasive temperature sensing of fluid passing through ⅜-in. medical plastic tubing, the design team I was working with selected a miniature infrared optical temperature sensor. The cylindrical sensor measured ¼ in. in diameter by 1 in. long. The sensor had a 1-to-1 field of view. The tubing we needed to sense was within the disposable component of the system. The sensor, spring-loaded to maintain slight pressure against the tubing when the disposable was clamped to the device, was centered on a U-shaped channel on the device to align with and "receive" the tubing.

We used the "heat-balance" method that the vendor recommended to accomplish temperature sensing. This method requires pressing the tubing against the sensor, which permits the sensor to convert the infrared energy that the fluid emits but ignores the effects of the tubing material or the disposable housing. To our surprise, this method seemed to work well in early breadboarding experiments to track the actual temperature, which we measured using standard thermocouples in contact with the fluid within a ±1°C tolerance of error. The method also tracked rapid changes in the fluid's temperature with only a few seconds of delay.

The vendor advertised that the sensor behaves as a K-type thermocouple at 37°C and is relatively accurate within our temperature range of interest: 10 to 50°C. In other words, its output should resemble the output of a contact thermocouple at the same temperature. We implemented a "cookbook" input circuit for a standard K-type thermocouple, expecting that it would perform perfectly. The breadboard prototype performed well, requiring only the addition of an offset adjustment to compensate for variations in components. We used the same conditioning circuit in the final design for both the optical infrared sensors and the standard-contact thermocouple sensors.

Once we implemented the design in the device, we noticed some odd behavior. With all sensors reading correctly and temperatures stabilized throughout the system, the optical thermocouples' output would rise significantly to as much as 5°C higher if anyone approached or touched any of the exposed metal parts on the device. The manufacturing operators also had a difficult time of adjusting the offset circuit for the infrared sensors with any repeatability, a fact that was no doubt related to the sensor's undocumented "proximity-sensing feature." The standard-contact thermocouple outputs did not change. This situation was, of course, unacceptable. A lot of head-scratching ensued!

After some investigation, we discovered that the optical infrared sensors had a measured impedance across their leads of nearly 20 kΩ! A standard thermocouple would normally appear as a short circuit. Apparently, this mismatch of impedance at the output of the infrared sensor and the input of the conditioning circuit was amplifying any minute sources of noise—in this case, induced ground noise—to an untenable level.

The cure was to place a 20-kΩ resistor across the input leads of the conditioning circuits of only the optical infrared sensors. The proximity-sensing feature and the difficulty in adjustment of the offset circuits miraculously disappeared! A review of the optical-sensor data sheets confirmed that they never mentioned this "output impedance." I suppose, in this case, a K-type "thermocouple" wasn't really a K-type thermocouple. EDN

Ken Whiteleather is a senior electrical engineer for Sparton Corp. Like Ken, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.


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Exploring the foundation under smartphones

The next generation of smartphones and PDAs will rely on unprecedented integration to deliver their features at the lowest possible bill-of-materials cost. But that doesn't mean they will be single-chip devices. Far from it: Radio chips, baseband processors, and application processors are likely to remain in separate packages. Around that core, a community of memory, support, and interface chips threatens to spring up and choke off the hope of cost control. To get an idea of the complexity of these hardware platforms and the challenge that integrators face, *EDN* looked into a smartphone/PDA reference-design board from Sophia Systems, which the company based on the Marvell PXA320 (codename, "Monahans") integrated application processor. Remember: This board contains no radio or baseband hardware, and the chip it uses contains L2 cache, a DDR DRAM controller, a 2-D-graphics engine, a 768-kbyte frame buffer, an LCD controller, a camera interface, and a host of I/O controllers.

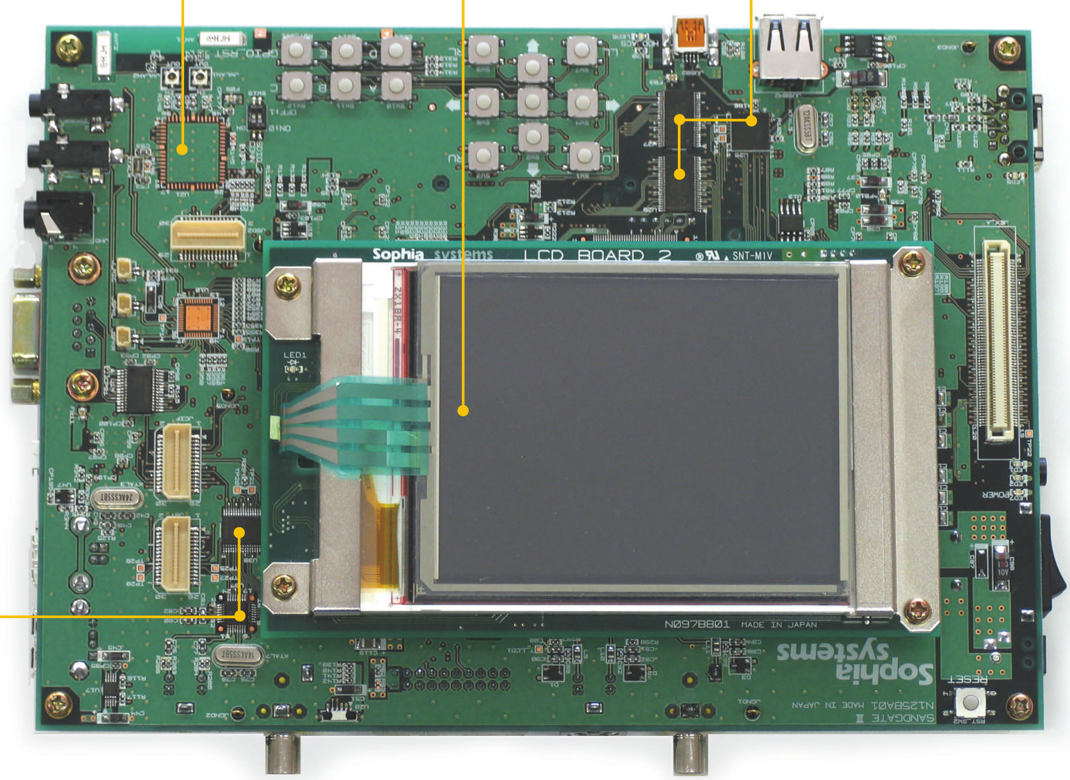
Despite all the I/O capabilities of the Monahans, the board still requires an Epson USB2.0/IDE controller, this pair of NXP 74ALVC164345 3/5V translators, and several other large packages of translation logic. Using multiple voltages saves power, but it quickly populates a motherboard with voltage shifters.

Monahans still requires an external Ethernet controller—in this case, an SMSC 9118 and a Pulse H1066 on the back of the board. There's a landing for a Murata WLAN module, as well.

The board comes with an LCD and touchscreen. Underneath the panel lies the heart of the design: the PXA320 Monahans CPU chip, 64 Mbytes of NAND flash, and 128 Mbytes of DRAM.

Power management is complex. This system provides a CPLD (on a daughtercard on the back of the board) to handle the complexities of power sequencing.

A TI TVP5150 decodes NTSC or PAL video to BT.656 digital data, and a Chrontel 7013 encoder provides the complementary function. More bus translation is necessary here, too.



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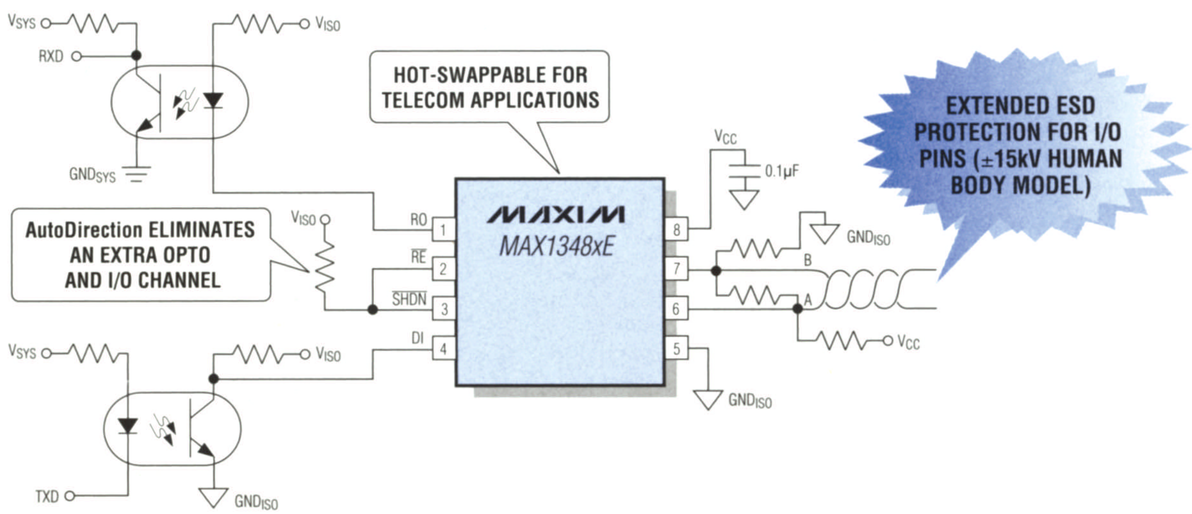

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MAX13487E		500	✔		8-SO
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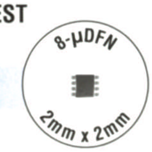

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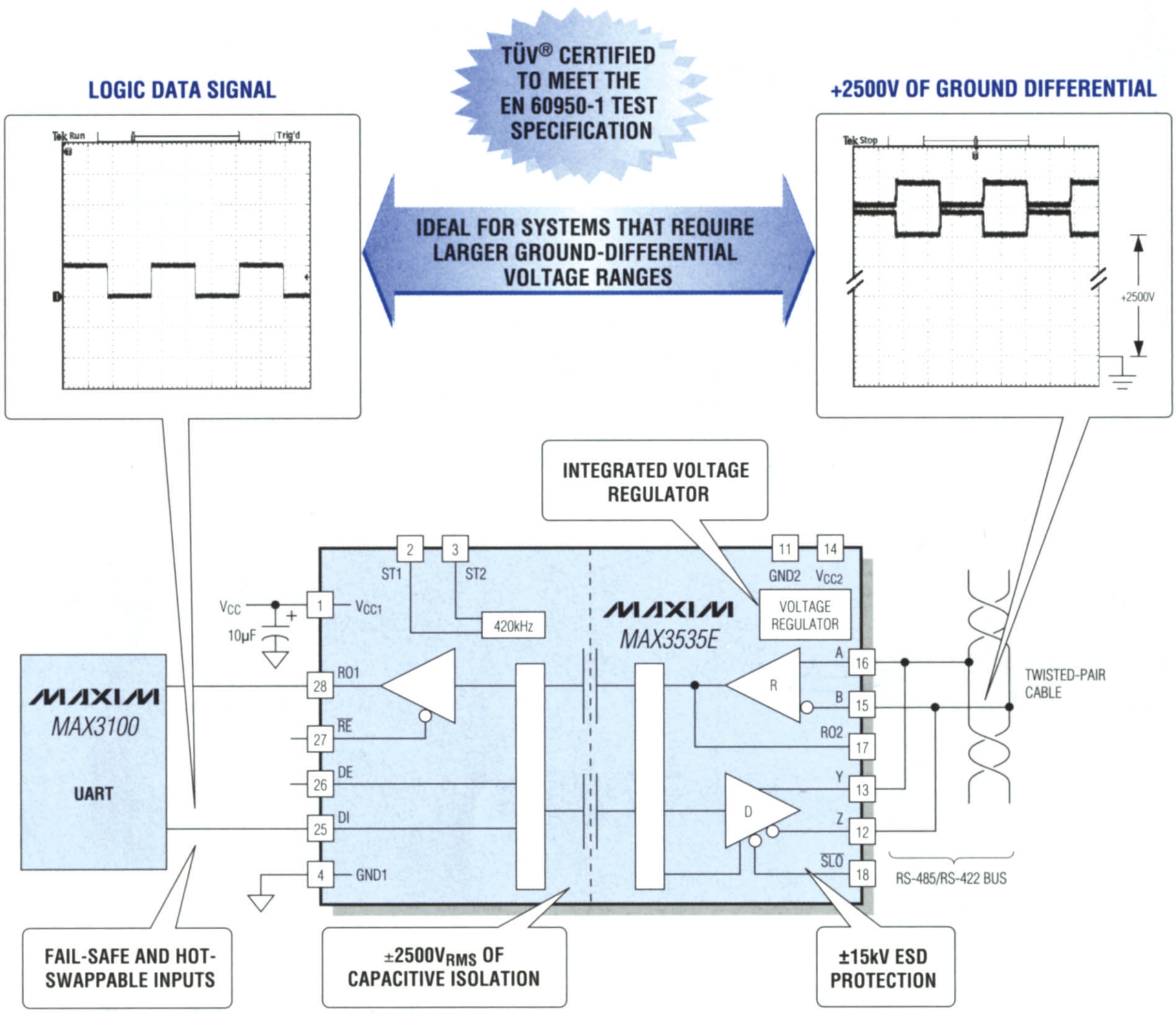
†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

DALLAS SEMICONDUCTOR MAXIM

Isolated RS-485 Transceiver

Industry's First +3.3V Isolated RS-485 Transceiver

Internal, Capacitive Isolation Barrier Provides Up to ±2500V_{RMS} of Isolation; Transmitter Outputs and Receiver Inputs Are Protected Up to ±15kV ESD



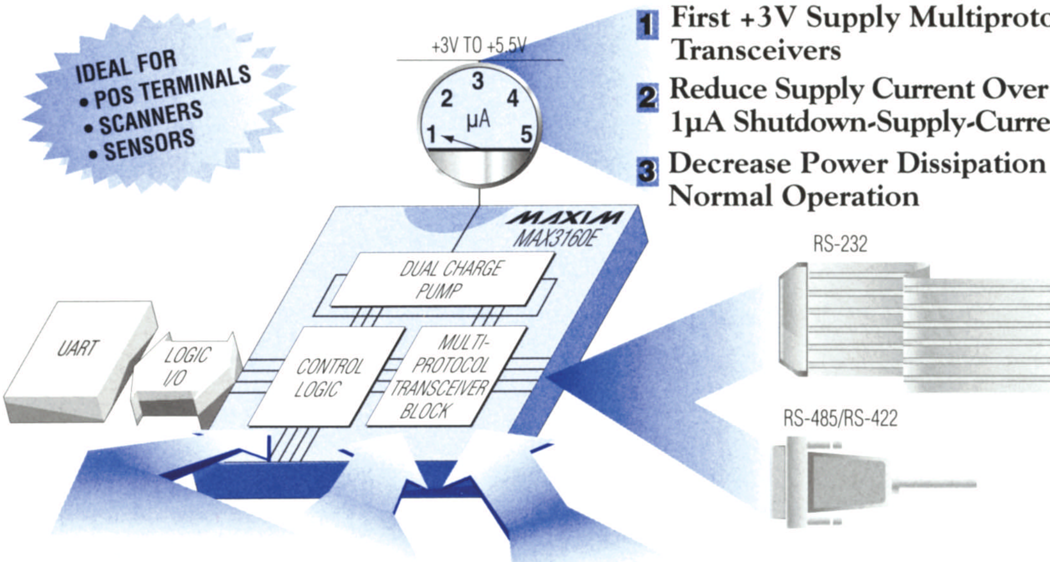
Eliminates the Need for External Optocouplers

Part	V_{CC} Supply (V)	Data Rate (kbps, max)	Isolation (V_{RMS})	±15kV ESD Protection	Hot-Swappable	Fail-Safe
MAX3535E	+3 to +5.5	1000	2500	✓	✓	✓

First 3V, ±15kV ESD, 1μA RS-232 and RS-485 Multiprotocol Interface Solutions

Multiprotocol Transceivers

MAX3160E FAMILY BEATS THE COMPETITION IN 9 WAYS



1. First +3V Supply Multiprotocol Transceivers
2. Reduce Supply Current Over 5x with 1μA Shutdown-Supply-Current Mode
3. Decrease Power Dissipation 4x in Normal Operation
4. Reduce EMI with Pin-Programmable Slew-Rate Limiting
5. Fastest RS-485 Data Rate (10Mbps) and RS-232 Data Rate (1Mbps)
6. Only Multiprotocol Transceivers on the Market with Pin-Programmable Half- or Full-Duplex Operation (MAX3160E/MAX3161E)
7. True Fail-Safe RS-485/RS-422 Receivers Guarantee a Logic 1 in Open- or Short-Circuit Conditions, Eliminating Framing Faults
8. 1/8-Unit Load Transceivers (MAX3161E/MAX3162E) Allow Up to 256 Transceivers on the Bus vs. Industry-Standard 32
9. ±15kV ESD Protection (Human Body Model)

Part	Interface Protocol	No. of Tranceivers on Bus	Package	Price† ($)
MAX3160E	Pin-programmable 2Tx/2Rx RS-232 or 1Tx/1Rx RS-485/RS-422	128	20-SSOP	5.94
MAX3161E	Pin-programmable 2Tx/2Rx RS-232 or 1Tx/1Rx RS-485/RS-422	256	24-SSOP	
MAX3162E	Dedicated 2Tx/2Rx RS-232 and 1Tx/1Rx RS-485/RS-422	256	28-SSOP	

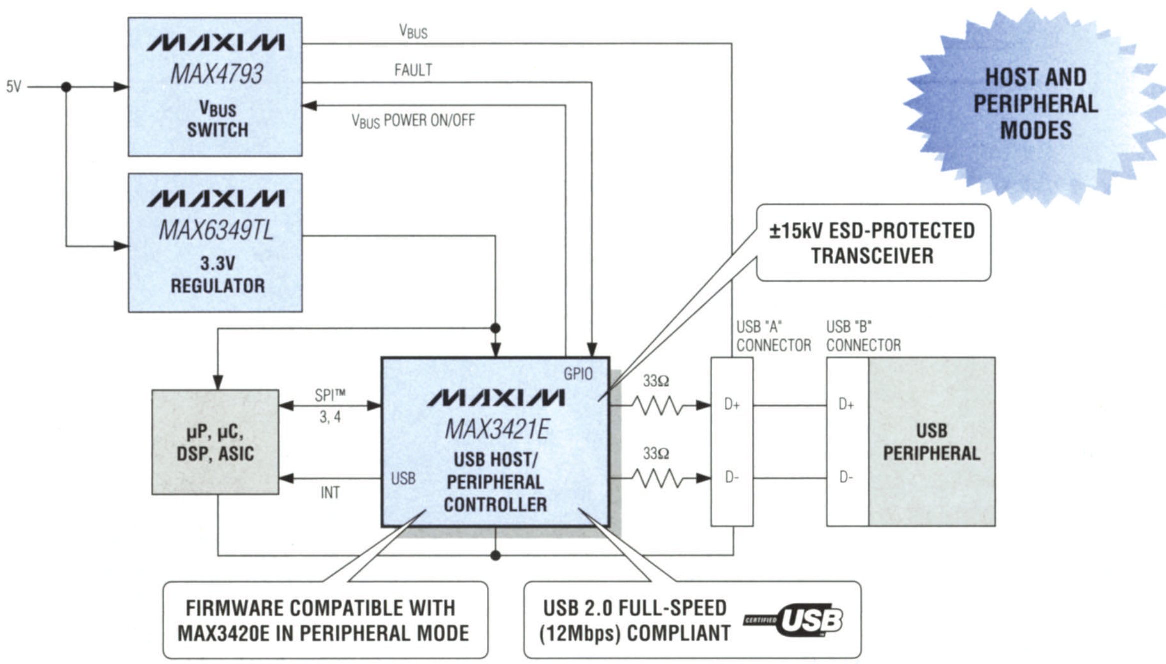
†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

USB Controllers

Add USB to *Any* System with a Single IC

Make Your µP, µC, DSP, or ASIC a Full-Speed USB Host/Peripheral

MAX3421E CONTROLLER ACTING AS AN EMBEDDED HOST



MAX3421E Features

- Host Capability in Addition to Peripheral Operation
- ±15kV ESD-Protected, Integrated Full-Speed USB Transceiver (12Mbps)
- SPI Interface to the Register Set (Up to 26MHz)
- Extra I/Os: 8 General-Purpose Inputs and 8 General-Purpose Outputs
- Low-Speed Host Operates Directly or Through USB Hub
- 5mm x 5mm, 32-Pin TQFN/TQFP
- Host Stack (Runs on ARM7) with Mass Storage Class Support

MAX3421E Ideal Applications

- Host—Connecting to USB Mice, Keyboards, Memory Sticks, Hub Support
- Peripherals—Industrial, Meter Reading, Automotive, Medical

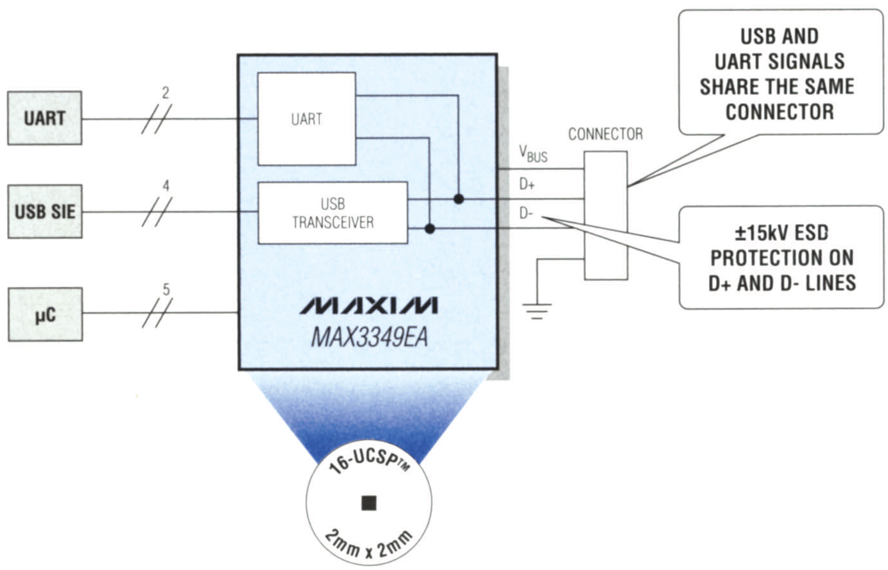
Part	Operation Mode	No. of General-Purpose Inputs	No. of General-Purpose Outputs	USB 2.0 Full-Speed (12Mbps) Compliant	Package (mm x mm)	Price† ($)
MAX3420E	Peripheral	4	4	✔	24-TQFN (4 x 4), 32-TQFP (7 x 7)	2.65
MAX3421E	Host or peripheral	8	8	✔	32-TQFN (5 x 5), 32-TQFP (5 x 5)	3.47

SPI is a trademark of Motorola, Inc.

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

±15kV USB Full-Speed Transceiver Has UART Multiplexer

Routes USB and UART Signals Through the Same Connector

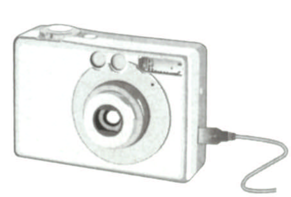


Features

- Integrated Functions Reduce System Component Count
- Switchable Pullup Resistor
- D+/D- Series Termination Resistors
- 5µA Low-Power Shutdown Mode
- Priced at $1.05†

Ideal Applications

- Cellular Handsets
- PDAs
- Digital Cameras
- MP3 Players

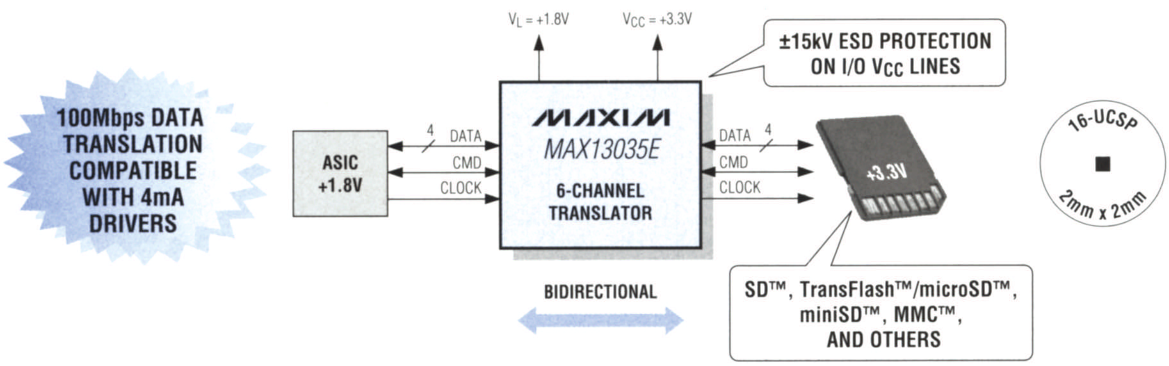


For Maxim's Full Line of USB Products, Go to:
www.maxim-ic.com/usb

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

Industry's Smallest Memory-Card Level Translator Requires No Data-Direction Pin

Translates Data Bidirectionally Up to 100Mbps



- High Data Rates with Minimal Drive Current
  - 100Mbps at 4mA
- Compatible with Push-Pull (CMOS) or Open-Drain Drivers
- ±15kV ESD Protection (I/O V_{CC})
- Bidirectional Data Translation
- No Data-Direction Pin Required
- Space-Saving, 2mm x 2mm UCSP Package
- AutoShutdown™ with $V_{CC} < V_L$ (MAX13035)

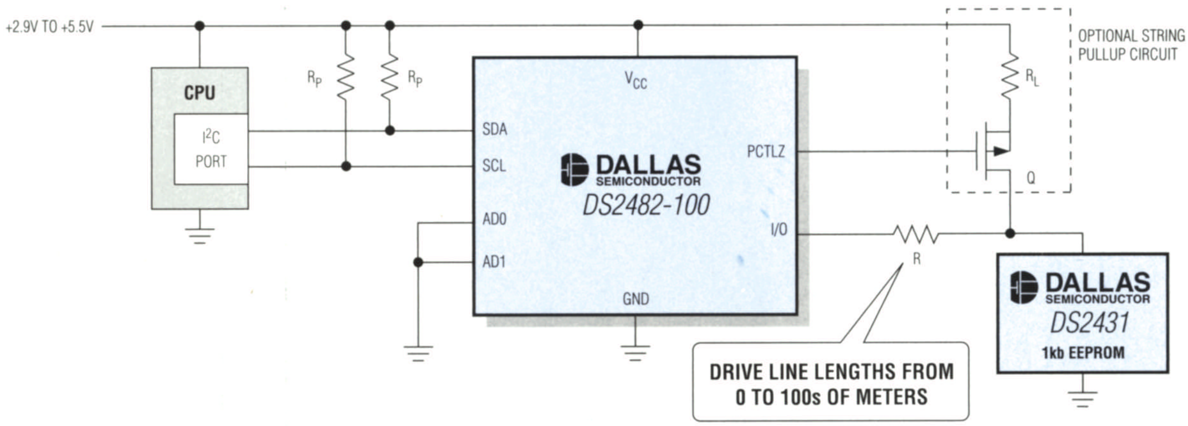
Part	No. of Channels	V_L Supply Voltage (V)	V_{CC} Supply Voltage (V)	I/O V_L Shutdown State	I/O V_{CC} Shutdown State	Data Rate (Mbps)	Package (mm x mm)	Price† ($)
MAX13030E	6	1.62 to 3.2	2.2 to 3.6	High impedance	High impedance	100	16-UCSP (2 x 2), 16-TQFN (4 x 4)	1.60
MAX13035E	6			75kΩ to V_L	High impedance		16-UCSP (2 x 2), 16-TQFN (4 x 4)	1.60
MAX13032E	6			High impedance	16.5kΩ to GND		16-UCSP	1.60
MAX13042E*	4				High impedance		12-TQFN (2 x 1.5)	—
MAX13043E*	4				16.5kΩ to GND		12-TQFN (2 x 1.5)	—

SD is a trademark of the SD Card Association.
TransFlash, microSD, miniSD, and MMC are trademarks of SanDisk Corporation.
AutoShutdown is a trademark of Maxim Integrated Products, Inc.
*Future product—contact factory for availability.
†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

Integrated Solutions for 1-Wire Host-Interface Designs

High-Level Command Capability, Reduced Hardware/Software Development Task, Optimized Line-Driving

The hardware implementation of a 1-Wire bus master can be accomplished with something as basic as a spare microcontroller port pin and a pullup resistor. Software bit-bangs the port pin to implement the 1-Wire protocol and read/write to slave devices. Another approach uses one of several 1-Wire line drivers that perform protocol conversion from a variety of serial or memory-mapped interfaces and provide high-level 1-Wire command capability. These devices can be used to greatly simplify the hardware/software development task necessary with discrete solutions. They also provide optimized 1-Wire waveform generation.



- **Regular and Overdrive 1-Wire Communication Speeds**
- **I²C, RS-232, USB 1.1 Memory-Mapped Host Interfaces**
- **High-Level 1-Wire Command Sequences**
- **Edge Control of 1-Wire Waveforms, Extending Communication Distance to Hundreds of Meters (Regular Speed Only)**
- **Low-Impedance, Strong Pullup for Slaves with Momentary High Source-Current Modes**
- **Resistive or Active 1-Wire Pullup**
- **Wide Operating Ranges: +2.9V to +5.25V, -40°C to +85°C**
- **Presence Pulse Masking (DS2482)**
- **Verilog®/VHDL Solution for ASIC/FPGA**

1-Wire Line Drivers

Base Part	Features
DS2480B	UART/RS-232-to-1-Wire protocol converter, provides a single 1-Wire bus master I/O port
DS2482-100	I²C-to-1-Wire protocol converter, provides a single 1-Wire bus master I/O port
DS2482-800	I²C-to-1-Wire protocol converter, provides eight 1-Wire bus master I/O ports
DS2490	USB-to-1-Wire protocol converter, 12Mbps USB 1.1, provides a single 1-Wire bus master I/O port
DS1482	Single-bit operation, +3.3V host to +5V 1-Wire level shifting, 1-Wire load sensing
DS1WM	Verilog or VHDL core implements 1-Wire bus master
DS9502/DS9503	ESD-protection diodes, ±25kV (typ) Human Body Model

Verilog is a registered trademark of Cadence Design Systems, Inc.

Interface Products

Part	V_{CC} Supply Voltage (V)	Fault Protection (V)	AutoShutdown	Data Rate (kbps)	Shutdown Supply Current (µA)	Fault Tolerant	Features
CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS							
MAX3050/3053	4.5 to 5.5	±80	✔	2000	15		Slope control, autowakeup
MAX3051	3 to 3.6	—		1000	5		3V supply, standby mode
MAX3054/3055/3056	4.5 to 5.5	±80/—/—		250/125/40	3	✔	Full wakeup, bus-failure detection
MAX3057/3058	4.5 to 5.5	±80		2000/1000	3/5		Slope control (MAX3057), standby mode
MAX3059	4.5 to 5.5	—		1000	10		Switched termination resistor
MAX13051/13052	4.5 to 5.5	±80	✔	1000	15		Autobaud (MAX13051), ±12V common-mode range

Part	Power Supply (V)	V_{CC} Supply Current (mA)	V_L Supply Current (mA)	USB Speed Supported	Features
USB CONTROLLERS					
MAX3420E	3 to 3.6	15	6	Full	±15kV ESD-protected, peripheral controller
MAX3421E	3 to 3.6	45	10	Full	±15kV ESD-protected, host and peripheral controller

Part	Power Supply (V)	Supply Current (mA)	Suspend Supply Current (µA)	USB Level Detect	Enumerate	USB Speed Supported	Features
USB TRANSCEIVERS							
MAX3344E*/3345E*	4 to 5.5	10	40	✔	✔	Full	±15kV ESD protection, internal 1.5kΩ pullup resistor, UCSP
MAX3346E*	4 to 5.5	8	40		✔	Low/full	±15kV ESD protection, internal 1.5kΩ pullup resistor, UCSP
MAX3453E	4 to 5.5	10	40	✔	✔	Full	±15kV ESD protection, internal 1.5kΩ pullup resistor
MAX3454E	3 to 5.5	10	35		✔	Low/full	±15kV ESD protection, internal 1.5kΩ pullup resistor
MAX3455E	4 to 5.5	10	35	✔		Low/full	±15kV ESD protection
MAX3456E	3 to 5.5	10	40			Low/full	±15kV ESD protection, pin compatible with MIC2550A
MAX13481E/2E	4 to 5.5	10	35	—/✔	✔	Full	±15kV ESD protection, internal 1.5kΩ pullup resistor (MAX13482E)
MAX13483E	4 to 5.5	10	35	✔		Full	±15kV ESD protection, V_{BUS} detection
MAX3349E	4 to 5.5	10	65	✔	✔	Full	Multiplexed USB and UART lines, ±15kV ESD protection, internal 1.5kΩ pullup resistor and series resistors
MAX3301E/3302E	3 to 4.5	10	500	✔		Full	±15kV ESD-protected, USB on-the-go (OTG) transceivers

Part	Power Supply (V)	Supply Current (mA)	Low-Power Shutdown (µA)	Receive FIFO Width (words)	Timing Compatible	Data Rate (kbps)	Package	Features
SPI/MICROWIRE™ UART								
MAX3100	2.7 to 5.5	150	10	8	✔	230	16-QSOP	9-bit address-recognition interrupt, receive-activity interrupt shutdown
INTEGRATED UART AND RS-232 TRANSCEIVERS								
MAX3110E	3 to 3.6	270	20	8	✔	230	28-SO	Combination UART and ±15kV ESD, RS-232 with internal capacitors
MAX3111E	4.5 to 5.5	150	20	8	✔	230	28-SO	Combination UART and ±15kV ESD, RS-232 with internal capacitors

Part	Power Supply (V)	No. of Tx/Rx	±15kV ESD Protection	Supply Current (1µA)	AutoShutdown Plus™	AutoShutdown	External Capacitors (µF)	Shutdown and Tristate	Rx Active in Shutdown	Data Rate (bps)
RS-232 INTERFACE PRODUCTS										
MAX3180E/3181E	3 to 5.5	0/1	✔	✔			—	✔ (MAX3180E)	✔ (MAX3181E)	1.5M
MAX3182E/3183E	3 to 5.5	0/1	✔	✔			—	✔ (MAX3182E)	✔ (MAX3183E)	1.5M
MAX3188E/3189E	±4.5 to ±6	1/0	✔			✔	—	✔		250k/1M
MAX3190E	±7 to ±12	1/0	✔			✔	—	✔		460k
MAX3209E	3 to 5.5, 12	6/10	✔			✔	2 x 0.1	✔	✔	460k
MAX3212	2.7 to 3.6	3/5		✔		✔	0.33/0.68	✔	✔	235k
MAX3218	1.8 to 4.25	2/2		✔		✔	0.33/0.68	✔	✔	120k
MAX3221E	3 to 5.5	1/1	✔	✔		✔	4 x 0.1	✔	✔	250k
MAX3222E/3223E	3 to 5.5	2/2	—/✔		—/✔		4 x 0.1	✔	✔	250k
MAX3224E/3225E	3 to 5.5	2/2	✔	✔	✔		4 x 0.1	✔	✔	250k/1M
MAX3226E/3227E	3 to 5.5	1/1	✔	✔	✔		4 x 0.1	✔	✔	250k/1M
MAX3228E*/3230E*	2.35 to 5.5	2/2	✔	✔		✔	4 x 0.1	✔		250k
MAX3229E*/3231E*	2.35 to 5.5	1/1	✔	✔		✔	4 x 0.1	✔		250k
MAX3232E/3233E	3 to 5.5/3.6	2/2	✔	—/✔	—/✔		4 x 0.1/—	—/✔	—/✔	250k
MAX3237E/3238E	3 to 5.5	5/3	✔	✔	—/✔		4 x 0.1	✔	✔	1M/250k
MAX3241E/3243E	3 to 5.5	3/5	✔	—/✔		—/✔	4 x 0.1	✔	✔	250k
MAX3244E/3245E	3 to 5.5	3/5	✔	✔	✔		4 x 0.1	✔	✔	250k/1M
MAX3246E*	3 to 5.5	3/5	✔	✔		✔	4 x 0.1	✔	✔	250k

*UCSP offered.

Interface Products (continued)

Part	Power Supply (V)	No. of Tx/Rx	±15kV ESD Protection	Supply Current (1µA)	AutoShutdown Plus	AutoShutdown	External Capacitors (µF)	Shutdown and Tristate	Rx Active in Shutdown	Data Rate (bps)
RS-232 INTERFACE PRODUCTS (continued)										
MAX3248E	3 to 5.5	5/3	✔	✔	✔		4 x 0.1	✔	✔	250k
MAX3311E/3313E	5	1/1					3 x 0.1			460k
MAX3314E	±5	1/1	✔				—			460k
MAX3322E	3 to 5.5	2/2	✔	✔			4 x 0.1	✔		250k
MAX3323E	3 to 5.5	1/1	✔	✔			4 x 0.1	✔		250k
MAX3325	3 to 3.6	2/2		✔			4 x 0.22	✔	✔	250k
MAX3380E/3381E	2.5 to 5.5	2/2	✔	✔	✔	✔	4 x 0.1	✔		250k
MAX3384E/3385E	3 to 5.5	2/2	✔	✔			4 x 0.1	✔	—/✔	250k
MAX3386E	3 to 5.5	3/2	✔	✔	✔		4 x 0.1	✔	✔	230k
MAX3387E	3 to 5.5	3/3	✔	✔	✔		4 x 0.1	✔	✔	250k
MAX3388E	2.35 to 3	3/2	✔	✔			4 x 0.1	✔		460k

Part	Power Supply (V)	No. of RS-232 Tx/Rx	Nom Reset Threshold (V)	Reset Pulse Width (ms, min)	$\overline{RESET}$ Valid to V_{CC} = 1V	Supply Current (µA)	No. of External Capacitors	Nom Capacitor Value (µF)	Shutdown and Tristate	Rx Active in Shutdown	AutoShutdown Plus	Data Rate (kbps)
INTEGRATED µP SUPERVISORS AND RS-232 TRANSCEIVERS												
MAX3320A/B/L/T	3 to 5.5	2/2	4.25/2.85/4.63/3.08	100	✔	✔	4	0.1	✔	✔	✔	250

Part	Power Supply (V)	Data Rate (kbps)	No. of Tx/Rx	Supply Current (mA)	Isolation Voltage (V)	Shutdown Supply Current (µA)	Features
ISOLATION PRODUCT (RS-232)							
MAX3250	3 to 5.5	250	2/2	15	±50	20	Surface-mount isolation, no external transformer needed

RS-485/RS-422 Products

Part	Power Supply (V)	No. of RS-485 Tx/Rx	Duplex	Data Rate (Mbps)	No. of Tx/Rx on Bus	Features
PREEMPHASIS FOR LONG DISTANCE AND HIGH SPEED						
MAX3291	5	1/1	Full	5 to 10	128	Pin compatible with industry standards
MAX3292	5	1/1	Full	Programmable	128	Pin compatible with industry standards

Part	Power Supply (V)	Supply Current (µA)	No. of RS-485 Tx/Rx	Duplex	Data Rate (kbps)	True Fail-Safe	1/8-Unit Load	Features
BATTERY POWERED (2.5V, 1.6µA)								
MAX3471	2.5 to 5.5	1.6	1/1	Half	64	✔	✔	Ideal for lithium battery-powered applications

Part	Data Rate (Mbps)	No. of RS-485 Tx/Rx	±15kV ESD Protection	Supply Current (mA)	Shutdown Supply Current (nA)	Duplex	No. of Tx/Rx on Bus	Features
3V SUPPLY (3.0V TO 3.6V)								
MAX3030E	20	4/0	✔	0.1	—	—	—	Pin compatible with 26LS31
MAX3031E	2	4/0	✔	0.1	—	—	—	Pin compatible with 26LS31
MAX3032E	20	4/0	✔	0.1	—	—	—	Pin compatible with 75174, 34C87
MAX3033E	2	4/0	✔	0.1	—	—	—	Pin compatible with 75174, 34C87
MAX3077E	16	1/1	✔	0.8	—	Full	256	True fail-safe receiver, hot-swap capable
MAX3094E/3096	10	0/4	✔	2.4	1	—	128	Rugged RS-422/RS-485 bus receiver
MAX3097E/3098EA	32	0/3	✔	3.1	—	—	256	32Mbps, four fault outputs
MAX3098EB	32	0/3	✔	3.1	—	—	256	32Mbps, four fault outputs
MAX3280E–3284E	52	0/1	✔	9	—	—	128	True fail-safe RS-485 in SOT23
MAX3362	20	1/1		1.7	1µA	Half	256	High-speed RS-485 transceiver in SOT23
MAX3483E	0.25	1/1	✔	1	2	Half	32	Slew-rate limiting reduces EMI and reflections
MAX3485E	12	1/1	✔	1	2	Half	32	Guaranteed 12Mbps data rate
MAX3486E	2.5	1/1	✔	1	2	Half	32	Slew-rate limiting reduces EMI and reflections
MAX3293	0.25	1/0		5	1	—	256	6-SOT23, slew-rate limited, hot-swap inputs
MAX3294	2.5	1/0		5	1	—	256	6-SOT23, slew-rate limited, hot-swap inputs
MAX3295	20	1/0		5	1	—	256	6-SOT23, hot-swap inputs

RS-485/RS-422 Products (continued)

Part	Data Rate (Mbps)	No. of RS-485 Tx/Rx	±15kV ESD Protection	Supply Current (mA)	Shutdown Supply Current (nA)	Duplex	No. of Tx/Rx on Bus	Features
3V SUPPLY (3.0V TO 3.6V) (continued)								
MAX3488E	0.25	1/1	✔	1	—	Full	32	Slew-rate limiting reduces EMI and reflections
MAX3490E	12	1/1	✔	1	—	Full	32	Guaranteed 12Mbps data rate
MAX3491E	12	1/1	✔	1	2	Full	32	MAX3490 plus driver/receiver enable

Part	Data Rate (Mbps)	No. of RS-485 Tx/Rx	Supply Current (mA)	Shutdown Current (µA)	AutoDirection	Duplex	±15kV ESD Protection	Features
5V SUPPLY								
MAX13485E	0.5	1/1	4	10		Half	✔	8-µDFN (2mm x 2 mm)
MAX13486E	16	1/1	4	10		Half	✔	8-µDFN (2mm x 2 mm)
MAX13487E	0.5	1/1	4	10	✔	Half	✔	AutoDirection, 8-SO
MAX13488E	16	1/1	4	10	✔	Half	✔	AutoDirection, 8-SO

Part	Data Rate (Mbps)	No. of Tx/Rx	Supply Current (mA)	Hot-Swap	Shutdown Supply Current (nA)	Duplex	No. of Tx/Rx on Bus	Features
PROFIBUS								
MAX3465/3466	40	1/1	2.5	✔ (MAX3465)	1	Full	128	Complies with PROFIBUS specifications
MAX3467	40	1/1	2.5		—	Full	128	Complies with PROFIBUS specifications
MAX3468/3469	40	1/1	2.5	✔ (MAX3468)	1	Half	128	Complies with PROFIBUS specifications

Part	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Tx/Rx	ESD Voltage (kV)	Supply Current (mA)	Shutdown Current (nA)	No. of Tx/Rx on Bus	Features
QUAD Tx/Rx								
MAX3040/3043	5	0.25	4/0	±10	1.0	2	—	±10kV ESD protection, hot-swap for live insertion
MAX3041/3044	5	2.5	4/0	±10	1.0	2	—	±10kV ESD protection, hot-swap for live insertion
MAX3042/3045	5	20	4/0	±10	1.0	2	—	±10kV ESD protection, hot-swap for live insertion
MAX3093E/3095	5	10	0/4	±15	2.4	< 1	128	5V, rugged RS-422/RS-485 bus receiver

Part	Standard	Power Supply (V)	Fault Protection (V)	Data Rate (Mbps)	No. of Tx/Rx	±15kV ESD Protection	Supply Current (mA)	Duplex	No. of Tx/Rx on Bus
FAULT-PROTECTED RS-485/RS-422/J1708									
MAX3430/13442E/13443E	RS-485	5	80	0.25	1/1	✔	30	Half	128
MAX3440E/3441E	RS-485	5	60	10	1/1	✔	10	Half	128
MAX13444E	J1708	5	80	0.25	1/1	✔	30	—	—

Part	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Tx/Rx	ESD Voltage (kV)	Supply Current (mA)	Shutdown Supply Current (µA)	Duplex	No. of Tx/Rx on Bus	Hot-Swap
TRUE FAIL-SAFE DEVICES									
MAX3070E/3073E/3076E	3 to 3.6	0.25/0.5/16	1/1	±15	0.8	0.05	Full	256	✔
MAX3071E/3074E/3077E	3 to 3.6	0.25/0.5/16	1/1	±15	0.8	—	Full	256	✔
MAX3072E/3075E/3078E	3 to 3.6	0.25/0.5/16	1/1	±15	0.8	0.05	Half	256	✔
MAX3079E	3 to 3.6	Selectable	1/1	±15	0.8	0.05	Selectable	256	✔
MAX13080E/13081E	5	0.250	1/1	±15	1.2	2.8/—	Full	256	
MAX13082E	5	0.250	1/1	±15	1.2	2.8	Half	256	
MAX13083E/13084E	5	0.5	1/1	±15	1.2	2.8/—	Full	256	
MAX13085E	5	0.5	1/1	±15	1.2	2.8	Half	256	
MAX13086E/13087E	5	16	1/1	±15	1.2	2.8/—	Full	256	
MAX13088E	5	16	1/1	±15	1.2	2.8	Half	256	
MAX13089E	5	Selectable	1/1	±15	1.2	2.8	Selectable	256	
MAX3093E/3095	5	10	0/4	±15	2.4	< 1nA	—	128	

Part	Power Supply (V)	Data Rate (Mbps)	No. of Tx/Rx	Supply Current (mA)	Isolation (V_{RMS})	Shutdown Supply Current (µA)	Full Duplex	Features
ISOLATION PRODUCTS (RS-485/RS-422)								
MAX3535E	3 to 5.5	1	1/1	100	2500	—	✔	3V to 5V supply operation, ±15kV ESD protection
MXL1535	5	0.25	1/1	100	2500	—	✔	±15kV ESD protection
MAX1480A	5	2.5	1/1	60	1600	0.2		Complete, isolated RS-485/RS-422 in one package
MAX1480B	5	0.25	1/1	35	1600	0.2		Complete, isolated RS-485/RS-422 in one package
MAX1480C	5	0.25	1/1	35	1600	0.2		MAX1480B with 1.5µs enable
MAX1490A	5	2.5	1/1	100	1600	0.2	✔	Complete, isolated RS-485/RS-422 in one package
MAX1490B	5	0.25	1/1	65	1600	0.2	✔	Complete, isolated RS-485/RS-422 in one package
MAX3480A	3.3	2.5	1/1	180	1600	0.2		Complete, isolated RS-485/RS-422 in one package

RS-485/RS-422 Products (continued)

ISOLATION PRODUCTS (RS-485/RS-422) (continued)

Part	Power Supply (V)	Data Rate (Mbps)	No. of Tx/Rx	Supply Current (mA)	Isolation Voltage (V_{RMS})	Shutdown Supply Current (µA)	Full Duplex	Features
MAX3480B	3.3	0.25	1/1	120	1500	0.2	—	Complete, isolated RS-485/RS-422 in one package
MAX3157	5	0.25	1/1	25	50	25	Selectable	Surface mount, no transformers required

RS-232/RS-485 MULTIPROTOCOL TRANSCEIVERS

Part	Supply Voltage (V)	No. of RS-232 Tx/Rx	No. of RS-485 Tx/Rx	RS-232/RS-485 Functionality	Half or Full Duplex	Fail-Safe	Data Rate	Supply Current (µA)	ESD Protection (kV)
MAX3160/3161	3 to 5.5	2/2	1/1	Pin programmable	Pin selectable	✔	Pin selectable	1	±15
MAX3162	3 to 5.5	2/2	1/1	Simultaneous	Full duplex	✔	Pin selectable	1	±15

MULTIPROTOCOL TRANSCEIVERS AND TERMINATION NETWORKS

Part	Supply Voltage (V)	No. of Transceivers	No. of Termination Networks	Protocols Supported	Selectable DCE/DTE	Package
MAX3170	3.3	3/3	—	V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, X.21), V.35	✔	28-SSOP
MAX3171/3173	3.3	3/3	—	V.28 (RS-232), V.10/V.11 (RS-449, V.36, EIA530, EIA530-A, X.21, RS-423)	✔	28-SSOP
MAX3172	3.3	1/1	5	V.28 (RS-232), V.11 (EIA530, EIA530-A, RS-449/V.36, X.21), V.35	✔	28-SSOP
MXL1543	5	3/3	—	V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, X.21), V.35	✔	28-SSOP
MXL1544	5	4/4	—	V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA530, EIA530-A, X.21, RS-423)	✔	28-SSOP
MXL1344A	5	—	6	V.28 (RS-232), V.11 (EIA530, EIA530-A, RS-449/V.36, X.21), V.35	✔	24-SSOP
MAX3174	3.3	1/1	5	V.11 (RS-422), RS-530, RS-530A, V.36/RS-449, V.35, V28/RS-232, V.10/RS-423, X.21)	✔	28-SSOP
MAX3175	5	4/4	—	V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA530, EIA530-A, X.21, RS-423)	✔	28-SSOP

LOGIC-LEVEL TRANSLATORS

Part	No. of V_L to V_{CC}/V_{CC} to V_L Translators	V_L Supply Range (V)	V_{CC} Supply Range (V)	V_{CC} Supply Current (µA)	Guaranteed Data Rate (bps)	ESD Protection (kV)	Pin-Controlled Shutdown	Features
MAX3000E/3001E	8/8	1.2 to 5.5	1.65 to 5.5	10	230k/4M	±15	✔	—
MAX3002	8/8	1.2 to 5.5	1.65 to 5.5	10	35M	—	✔	—
MAX3013	8/8	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	0.1	100M	—	✔	—
MAX13013/13014	1/1/2/2	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	0.1	100M	—	✔	—
MAX3023	4/4	1.2 to (V_{CC} - 0.4)	1.65 to 3.6	0.1	100M	—	✔	—
MAX3372E/3373E*	2/2	1.2 to 5.5	1.65 to 5.5	130	230k/6M	±15	✔	—
MAX3377E/3378E*	4/4	1.2 to 5.5	1.65 to 5.5	130	230k/6M	±15	✔	—
MAX3394E*	2/2	1.2 to 5.5	1.65 to 5.5	150	6M	±15	✔	Supports large capacitive loads
MAX3396E	2/2	1.2 to V_{CC}	1.65 to 5.5	150	6M	±15	✔	Supports large capacitive loads
MAX13000E-13005E*	6	0.9 to 3.6	1.5 to 3.6	40	230k/20M	±15	✔	—
MAX13102E/103E/108E	16/16	1.2 to V_{CC}	1.65 to 5.5	10	20M	±15	✔	Multiplexing option (MAX13108E)
MAX13035E	6/6	1.62 to 3.2	2.2 to 3.6	18	100M	±15	✔	Compatible with 4mA drivers

RS-232 TRANSCEIVER WITH SEPARATE LCD POWER AND BIAS

Part	Power Supply (V)	No. of Tx/Rx	LCD Contrast Voltage Range (V)	Shutdown Supply Current (µA)	External Capacitors (µF)	Shutdown and Tristate	Rx Active in Shutdown	Data Rate (kbps)
MAX3325	3 to 3.6	2/2	-5 to +2	1	4 x 0.22	✔	✔	250

TERMINATION ICs

Part	Supply Voltage Range (V)	Signal Range (V)	Termination Values (Ω)	Resistance Accuracy (%)
MAX3406	4.5 to 5.5	±3.6	100/75	±2.5
MAX3407	4.5 to 5.5	±3.6	120/75	±2.5
MAX3408	4.5 to 5.5	±3.6	100/120	±2.5

ESD-PROTECTION DEVICES

Part	Power Supply (V)	No. of ESD-Protection Channels	Input Capacitance (pF)	ESD Protection: ±15kV Human Body Model, ±8kV IEC 61000-4-2 Contact, ±15kV IEC 61000-4-2 Air-Gap	Supply Current (nA)
MAX3202E/3203E	0.9 to 5.5	2/3	5	✔	1
MAX3204E/3206E	0.9 to 5.5	4/6	5	✔	1
MAX3205E/3207E	0.9 to 5.5	6/2	2.5	✔	1
MAX3208E	0.9 to 5.5	4	2.6	✔	1
MAX13202E	0.9 to 16	2	6	±15kV (HBM), ±12kV (Contact), ±30kV (Air Gap)	1
MAX13204E/6E/8E	0.9 to 16	4/6/8	6	±15kV (HBM), ±14kV (Contact), ±30kV (Air Gap)	1

USB ON-THE-GO

Part	V_{CC} Supply Voltage (V)	V_L Supply Voltage (V)	±15kV ESD Protection	USB OTG Transceiver	V_{BUS} Supply and Signaling	Switchable D+/D- Resistors	Shutdown Supply Current (µA)
MAX3301E	3 to 4.5	1.65 to 3.6	✔	✔	✔	✔	3.5
MAX3353E*/3355E*	2.6 to 5.5/1.65 to 5.5	1.65 to V_{CC}	✔		✔	✔/—	0.4/1

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EDN's 2006 INNOVATOR/INNOVATION PROGRAM WINNERS

TO THE VICTOR GO THE STATUETTES

The competition for *EDN*'s 17th Annual Innovation Awards was fierce again this year. The contest drew contenders that ran the electronics-industry gamut—from digital technologies, to mixed-signal products, to processors and controllers. As always, *EDN* strives to recognize and honor the industry's most innovative technical advancements as well as the designers behind those innovations. These are the advances that touch every aspect of the way people live and work around the globe. Moreover, *EDN*, through its awards program, endeavors to foster the growth of engineering careers and the future of electronics through an annual contribution to engineering education. *EDN* awards this contribution to the Innovator of the Year, who, in turn, can donate it to the engineering school of his or her choice.

The 17th annual awards, like last year, took place at the 4th Street Summit Center in San Jose, CA, and helped kick off the busy Embedded Systems Conference week. At the April 2 shindig, *EDN* introduced some of its own innovations to the evening's program, including its new publisher, Alan Robinson, and the award-winning comedy and wizardry of Master of Ceremonies Bill Herz. Innovation winners took home (or at least back to the office) statuettes for 15 product and technology categories as well as for 2006's Best Contributed Article and Innovator of the Year.

Read on to learn who took top honors at this year's awards ceremony.
EDN **congratulates all the winners! To learn more about our Innovation program, visit www.edn.com/innovation.**

✦INNOVATOR OF THE YEAR

Steve Douglass, Suresh Menon, and the Virtex-5 LXT design team, Xilinx

A lot of product designs face a roadblock, but few face the number of obstacles that Steve Douglass, Suresh Menon, and the Xilinx Virtex-5 LXT design team did. The FPGA design included a move to a 65-nm process, necessitated a balance of programmability and hard-IP (intellectual-property) features, and realistically required a solution to ballooning dynamic-power consumption. The result is a chip that has more than 1 billion transistors, yet, according to Xilinx, it realized a 35% reduction in dynamic power relative to earlier 90-nm designs.

The Virtex-5 LXT team included more than 200 engineers organized into groups called Centers of Excellence, with each group focusing on one aspect of the new architecture. Product planners met with hundreds of system designers to get input on the new architecture. The company claims that the result is 30% higher performance and 65% higher logic density.

The Virtex-5 LXT design leads a trend of balanced programmability and fixed functions. The chip includes built-in hard-IP blocks for what Xilinx claims are the two most popular serial-I/O standards: PCIe (PCI Express) and Gigabit Ethernet. The hardened PCIe endpoint block saves users as many as 10,000 look-up tables and 2W of power compared with soft-IP-core implementations. The company points to industry research suggesting that PCIe and Gigabit Ethernet will account for approximately 80% of all I/O-port shipments in 2009, making a case for hardening these blocks on the FPGA, thus saving logic resources and consuming lower power than soft-IP approaches.

✦ANALOG ICs

Symphony Class D audio amplifier, Freescale Semiconductor

Conventional Class D audio amplifiers operate the PWM-output section open-loop, which makes the amplifier susceptible to power-supply variations. Even advanced Class D amplifiers have an only −40-dB spec on PSRR (power-supply-rejection ratio) at 60 Hz. The Freescale FSA95601 uses an innovative digital-feedback technique to achieve remarkable performance. It achieves THD (total harmonic distortion) of −120 dB and IMD (intermodulation distortion) of −110 dB. Open-loop systems require fast transitions at the output of the switching-power stage to achieve reasonable distortion performance. Fast switching transitions are detrimental to EMI (electromagnetic-interference) performance. The Freescale FSA95601 allows for slower transitions at the switching-power-stage output. Overall, this chip set represents a significant advancement in system-level Class D audio amplifiers.

Due to its immunity to power-supply variations, the first application for this chip set is in the automotive industry. The chips target applications requiring 50 to 100W (bridged) per channel. In addition, the chip set offers advanced protection features, such as undervoltage, overvoltage, and overtemperature warning, and it provides advanced turn-on/off audio click-and-pop suppression.

✦POWER ICs

IR1167 SmartRectifier IC, International Rectifier

There are relatively few ICs that manage power on the secondary side of an isolated supply. Although FETs have replaced diodes on modern synchronous buck converters, there has not been a similar effort to replace the diodes in the secondary of isolated supplies. International Rectifier's IR1167 SmartRectifier IC simplifies secondary SR (synchronous rectification) for ac/dc-power converters and improves power density for high-power flyback and resonant half-bridge converters, enabling smaller, cooler designs.

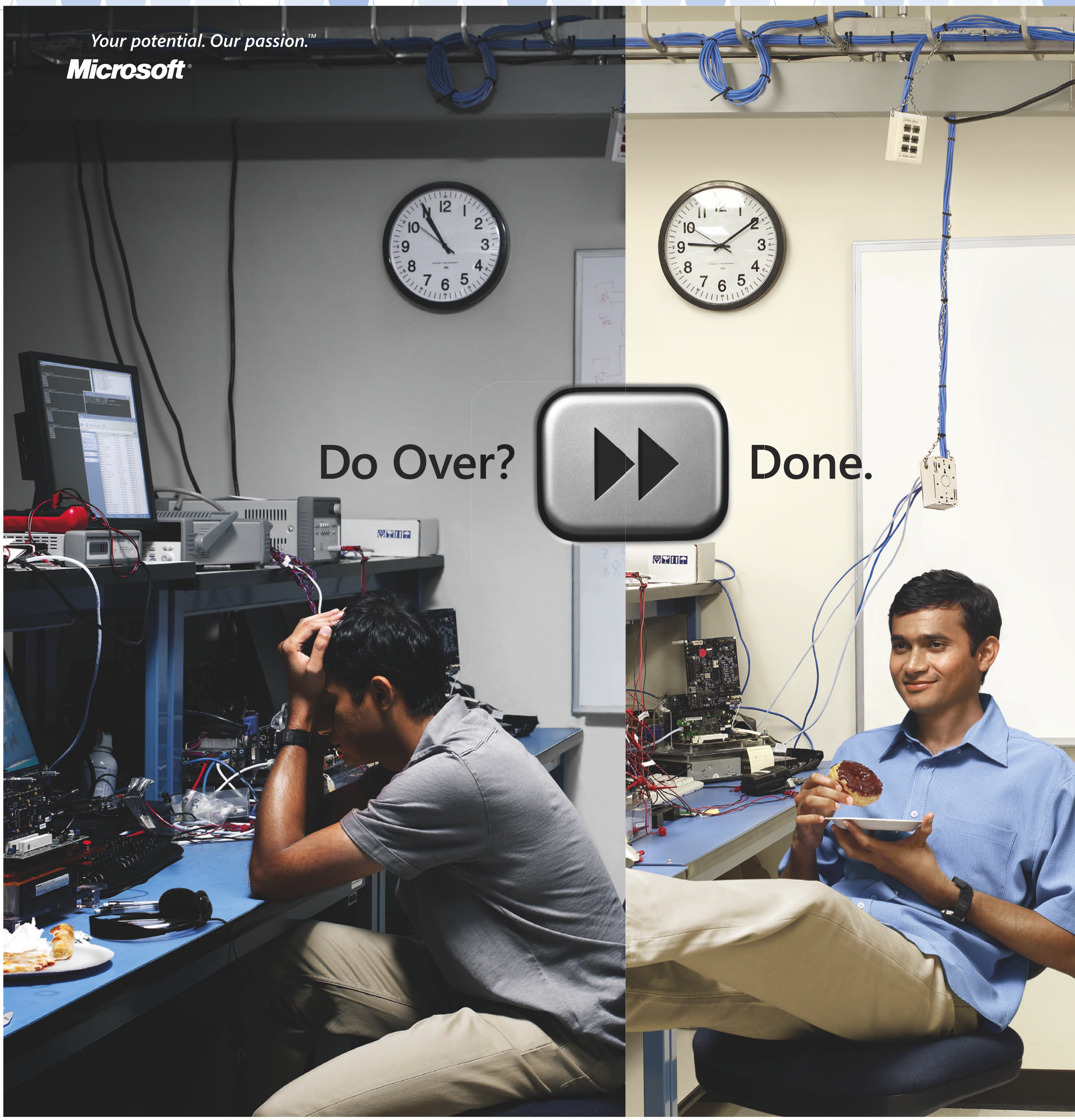
The IR1167 is independent of the primary-side controller. It uses IR's proprietary HVIC (high-voltage-IC) technology for directly sensing and controlling secondary-side rectification. In addition to controlling high-power flyback secondary sections, the SmartRectifier is the first commercial IC for resonant half-bridge converters. Compared with discrete-current-transformer-based designs, the IR1167 increases power-subsystem efficiency by at least 1%. Independence from the primary side means that the IR1167 operates in variable-frequency mode as well as at low-power burst modes.

✦MIXED-SIGNAL ASSPs

AKU2000 digital MEMS microphone, Akustica

It may seem strange, at first glance, to encounter a microphone as an Innovation Awards winner. After all, the materials that comprise ECMs (electret-condenser microphones) have existed since the 1920s, and Bell Laboratories unveiled the first practical ECM, basing it on thin metallized Teflon foil, in 1962. But leave it to Akustica, with the AKU2000, to bring vitality back into a moribund product category.

The core of Akustica's achievement is MEMS (microelectromechanical systems), a technology that to date has seen its broadest use in ink-jet print heads, optical switches, DLP (digital-light-processing) engines, accelerometers, gyroscopes, and pressure sensors. Unlike traditional MEMS devices, which require custom thin-film semiconductor techniques, Akustica's AKU2000 employs the



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metal-dielectric layers of conventional CMOS processes.

ECMs' analog outputs are susceptible to signal corruption from nearby EMI-radiating sources, such as cell phones, LCDs and their backlights, and Wi-Fi transceivers. As a result, engineers must often place them in nonideal locations to minimize cabling lengths to the system board and must also burden the system with the cost of shielding materials.

✦NETWORK AND COMMUNICATIONS ICs

QSC (Qualcomm Single Chip) solutions for CDMA2000 1X, Qualcomm

Qualcomm's QSC (Qualcomm Single Chip) product family includes the QSC6065, which it manufactures on a 65-nm process and designs to support gaming, multimedia, and location services. The IC supports 3M-pixel cameras with 15-frame/sec video recording and playback at QCIF (Quarter Common Intermediate Format) resolution. The 4GV dynamic voice-codec architecture allows carriers to prioritize voice quality or network capacity. Qualcomm claims that the location features it bases on a GPS (global-positioning system) allow for enhanced indoor and dense-urban-area performance by means of state-of-the-art −159-dBm GPS sensitivity. The design also supports concurrent voice and positioning operations, enabling seamless E911 calls and voice-based location services.

✦MULTIMEDIA ICs

LSI DMN-8633 single-chip media processor, LSI Logic

LSI Logic's DMN-8633 single-chip media processor decodes multimedia feeds originating from all 18 standard- and high-definition ATSC formats and other MPEG-2 transport-stream sources, along with DV-formatted data. To that end, the DMN-8633 incorporates both FireWire and 12-Mbps USB transceivers.

The DMN-8633 lets you transcode the audio/video streams on the fly to standard-definition video for recording onto a conventional red-laser DVD, in MPEG-4 Advanced Simple Profile, MPEG-4-derived DivX, and conventional MPEG-2 formats. Because you'd want a DMN-8633-based design to act also as a conventional DVD player, you'll be happy to know that the chip also supports the playback of DVD-Video disks with Dolby Digital 5.1, MPEG-1 Layer 2 or DTS (digital-theater-sound) audio tracks, and VCDs (video compact discs) and SVCDs (super-video CDs). The DMN-8633 also decodes JPEG images, along with DVD-Audio (Multilink Point-to-Point Protocol), WMA (Windows Media Audio), and CD-DA (compact-disc digital-audio) audio bit streams. Progressive-scan analog-video (both component and RGB) and digital-video outputs come standard. The digital-video outputs automatically scale up to high-definition resolutions. The chip's integrated video encoder also simultaneously supports S- and composite-video connections. The DMN-8633 costs $20 (1 million); the higher end $25 DMN-8683 supports two MPEG-2 transport-stream inputs for simultaneous record and playback applications, along with both hard-disk-drive- and DVD-stream-capture destinations.

✦DIGITAL ICs, PROGRAMMABLE LOGIC, AND MEMORY

Virtex-5 LXT FPGAs, Xilinx

In 2006, Xilinx was the first company to implement an FPGA in 65-nm silicon. Later in the year, the company introduced the LTX version of its Virtex-5, which combines the performance, power, and cost advantages that 65-nm technology brings to a programmable-logic fabric with built-in hard-IP (intellectual-property) blocks for the two most popular serial-I/O standards: PCIe and Gigabit Ethernet. As such, Xilinx says, the Virtex-5 LXT FPGAs are poised to address the SOC (system-on-chip) requirements for the triple-play (voice-, video-, and data-services) infrastructure market and meet challenging bandwidth, power, and cost targets.

Virtex-5 LXT devices increase performance by an average of 30%, increase capacity by 65%, and reduce dynamic power consumption by as much as 35% over previous-generation 90-nm FPGAs. The hardened PCIe endpoint block saves users as many as 10,000 look-up tables and 2W of power compared with soft-IP-core implementations.

✦MICROCONTROLLERS AND DSCs

TMS320F28044 DSC, Texas Instruments

The TMS320F28044 DSC (digital-signal controller) can manage as many as 16 dc/dc-converter channels for multiphase control. Texas Instruments' integrated HRPWM (high-resolution pulse-width-modulation) technology supports a 150-psec resolution for each channel.

Together, the DSP core, the HRPWM, and the 80-nsec ADC support the full digital-loop control and deliver output accuracy to enable switching frequencies over a single channel as fast as 1 MHz and over 16 channels as fast as 200 kHz.

✦MICROPROCESSORS AND DSPs

Core 2 Duo processor, Intel

Intel's 65-nm-silicon-process technology enables Intel's Core 2 Duo processors to deliver a 40% increase in performance and a more-than-40% improvement in energy efficiency versus Intel's previous best processor.

These dual-core devices benefit from a 14-stage pipeline in each core that can simultaneously complete as many as four instructions. The Smart Memory Access capability relies on "memory disambiguation," which better hides the latency of memory accesses by increasing the efficiency of out-of-order processing. It enables each core to speculatively load data for instructions that are about to execute before all previous store instructions execute.

✦EDA: ESL, PCB, AND IC FRONT-END TOOLS

Analog FastSPICE and RF FastSPICE simulators, Berkeley Design Automation

Berkeley Design Automation has come

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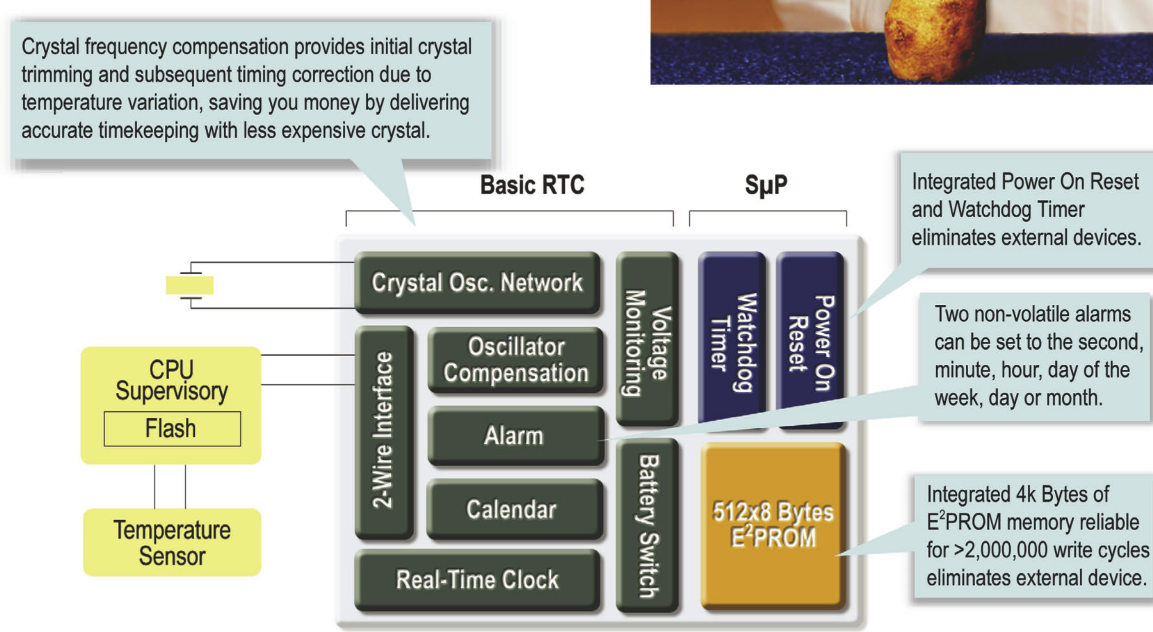

800nA General Purpose Real-Time Clock Selector Table

	Int. E²PROM (Bytes)	Alarm	CPU Sup.Fx's POR	CPU Sup.Fx's Wdg Timer	$\overline{IRQ}$	F_{OUT}	V_{TRIP} for Rest/Bat Switch	Package
ISL12026	512 X 8	2	N	N	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12027	512 X 8	2	Y	Y	$\overline{RESET}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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up with an innovative approach to speed SPICE simulation and maintain SPICE accuracy. The company claims both tools provide full-SPICE accuracy, five- to 10-times better performance than SPICE, and vastly superior dc and PSS (periodic-steady-state) convergence.

✦BEST CONTRIBUTED ARTICLE

"Signal conditioning for high-impedance sensors," by Glen Brisebois, Linear Technology

Maintaining accuracy in circuits that process signals from high-impedance sensors presents unique challenges. First, you need to identify when to use special design techniques. Then, you must choose devices that buffer and protect the sensors and circuits without destroying their accuracy.

✦EDA: IC BACK-END AND DFM TOOLS

Space-based Router, Cadence Design Systems

Cadence says today's conventional IC-implementation tools create an oversimplified model of interconnect and associated foundry-process rules. Cadence Space-based Router and Cadence Chip Optimizer use a patented 3-D, space-based approach to model and analyze true shapes and intervening physical spaces.

The technology allows engineers to position shapes and spaces in the exact configuration and location they need to correct subwavelength-manufacturing effects. This technology affords greater precision and flexibility when optimizing the interconnects and uses tiered design and manufacturing constraints.

✦COMPUTERS, BOARDS, AND BUSES

SkyeModule M9 embedded RFID reader, SkyeTek

Laying claim to the world's smallest globally compliant, UHF RFID-reader module, SkyeTek's SkyeModule M9 targets OEM embedded-system applications in asset tracking, access control, inventory management, and anticounterfeiting. Half the size of a typical business card, the M9 allows designers to choose the combination of tags, protocols, and hardware that best suits their applications. The M9 has fine-grain-controllable RF power from 10 to 500 mW, providing reliable read ranges beyond 2m. The module supports anticollision, dense-reader mode, and a broad array of EPC (Electronic Product Code) and ISO (International Standards Organization) tags.

SkyeTek's open-reader architecture allows upgrading of the M9 in the field to add postdeployment tags, protocols, and security through a firmware update.

✦SENSORS AND COMPONENTS

ADIS16250/iSensor intelligent sensor, Analog Devices

Motion-, or angular-rate-, sensing functions demand a significant investment of development time and design resources and require that system designers have a full understanding of the steps necessary to embed control features into the core.

Analog Devices' ADIS16250 iSensor intelligent sensors fill the gap between ultrahigh-performance, high-cost, fully integrated gyros, which have long seen use in military applications, and more recently available sensing options that achieve lower performance, accomplish less integration, and require significant knowledge of sensing design.

The ADIS16250 is the first MEMS (microelectromechanical) gyroscope to provide both digital range scaling and embedded programmability, eliminating a significant barrier to integrating gyroscopes into industrial systems. The single-chip ADIS1650, which leverages ADI's iMEMS motion-signal-processing technology, also uses less than half the board space of multicomponent products and delivers more advanced control functions.

✦POWER SOURCES

TurboTrans point-of-load power modules, Texas Instruments

Texas Instruments introduced its T2 series in November 2005 to reduce the amount of capacitance in high-transient power designs. These second-generation plated-through-hole modules, suitable for intermediate-bus applications, employ TurboTrans technology to allow power-supply designers to dynamically "tune" the modules using a single external resistor to meet a specific transient-load requirement with as much as eight times less capacitance.

✦SOFTWARE

Nios II C-to-hardware-acceleration compiler, Altera

Claiming to reduce development time from weeks to minutes, the Nios II C2H (C-to-hardware-acceleration) compiler development tool from Altera automatically converts time-critical ANSI C subroutines into hardware accelerators and integrates them into FPGA-based Nios II subsystems. C2H runs straight ANSI C and requires no special libraries or nonstandard C constructs.

✦TEST AND MEASUREMENT

Medalist bead-probe technology, Agilent Technologies

Agilent calls its bead-probe technology the industry's first proven technology for placing test targets directly on PCB (printed-circuit-board) signal traces. These beads then serve as highly reliable test points for use during ICT (in-circuit testing). This new technique dramatically improves ICT access on high-density and high-speed boards.

You create bead probes during PCB manufacturing by opening the solder mask and exposing the copper trace wherever you desire a test point. Once you apply solder paste along the trace and reflow it, you can readily probe the trace at ICT with flat-headed (not pointed) probes. The probe's spring force partially crushes the bead, removing any residual flux residue, and provides an excellent surface for electrical contact.

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V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

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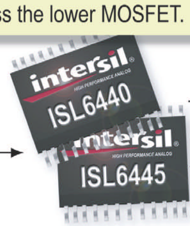
Triple Output PWM Controller
4.5V to 5.5V or 5.6V to 24V Input Voltage →

V_{OUT1}: **Adjustable, 0.8V to V_{IN}**
V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

An adjustable overcurrent protection circuit monitors the output current by sensing the voltage drop across the lower MOSFET.

Dual Output PWM Controller
4.5V to 5.5V or 5.6V to 24V Input Voltage →



V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

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EDN DSP DIRECTORY

ARE YOU TRYING TO KEEP TRACK OF THE CONSTANT CHANGES IN THE WORLD OF DIGITAL-SIGNAL-PROCESSING OFFERINGS? THE 2007 DIRECTORY CAN HELP.

THE BEST OF BOTH WORLDS

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

www.edn.com/dspdirectory

Welcome to the 2007 *EDN* DSP Directory, which again groups an ever-expanding list of digital-signal-processing resources into a single repository. The number of companies, devices, cores, and offerings in the directory continues to evolve and grow. A few companies have dropped out due to the closing of business or spin-offs, but the company roster and table of devices are always expanding. This steady growth are a testament not only to the variety of available processing options, but also to the tremendous variation among requirements, features, and applications for which designers use these devices and cores.

Last year, we proposed the term DSC (digital-signal controller) to describe the growing number of hybrid or unified architectures that consist of a microcontroller core with DSP-architecture features and structures. This year, we'd like to highlight this growing segment of the digital-signal-processing universe. DSCs differ from pure DSPs and microcontrollers in that they combine essential features of each type of processor into a single architecture, instruction flow, and device. They support more frequent and faster context switching by including a richer set of on-chip peripherals and interrupt controls than you find on pure DSPs. They also incorporate a richer bus structure and set of arithmetic-execution units for minimizing the chance of computational stalls that a pure microcontroller could suffer when processing a continuous stream of data, such as while processing context switches.

DSCs are making a range of new applications feasible as optimized devices with the right mix of peripherals and data processing integrated into application-specific devices. An early application target for these devices has been the power-supply controller. The balance between the dual nature of DSCs suits them for applications that need to be able to perform complex control functions and perform signal processing at the edges of a system or in small- or portable-system applications. Expect to see more application-specific DSCs for smart-building (automation) applications and portable devices—especially for portable home-medical equipment.

The directory continues to aim to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. This print version offers a quick and high-level overview of the digital-signal-processing industry by identifying what is new at each company and what applications each company's product lines target.

The DSP Directory is available online at www.edn.com/dspdirectory. There, the "Where did they go?" section helps you find companies that we no longer list because they are out of business, other companies have acquired them, or they've failed to supply us with the updated information we needed for this year's directory. The section also includes data from previous years to make tracking this type of data easier without having to locate earlier versions of the directory.

Further, the Web version expands greatly on the print edition. It offers not only the print material, but also device tables and detailed pages dedicated to each company's devices, cores, development tools, and other product offerings. The detailed device pages support a top-level taxonomy that allows you to find the devices by vendor and by application. These pages also include architectural block diagrams, if available, for each vendor's offerings.

If you cannot find a company in the directory or if a company did not participate in the update, please let the company and *EDN* know that you missed reading about it in the directory. Likewise, if this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to make the directory better by visiting us at www.edn.com/dspdirectory or by sending your comments and feedback to dspdirectory@edn.com.

ACTEL CORP, WWW.ACTEL.COM

Actel offers single-chip, nonvolatile FPGA technologies along with signal-processing capabilities, such as filtering and domain conversion. The company's Direct-Core system-level IP (intellectual-property) blocks target use with its FPGAs, such as the RTAX-S and ProASIC3 device families. When implemented in Actel's flash- and antifuse-based FPGAs, the flexible IP cores are immune to firm errors and tolerant of radiation. The company's devices support live-at-power-up, which allows them to target military, communication, aerospace, and medical applications that require no power-up delay.

The CoreCORDIC (coordinate-rotation-digital-computer) algorithm, which Actel introduced last year, calculates hyperbolic and trigonometric functions. It also performs coordinate transformations between rectangular and polar coordinates. The tool supports RTL generation, which enables designers to build configurable digital-signal-processing systems. CoreCORDIC supports three architectural options, including a small, bit-serial architecture, a word-serial architecture for moderate performance and size, and a parallel-pipelined architecture for high-performance applications. The CoreCORDIC generator creates a user-defined testbench and RTL model that easily integrates into larger designs. Actel also supports core generation with its CoreFIR (finite-impulse-response) and CoreFFT (fast-Fourier-transform) offerings.

ALTERA, WWW.ALTERA.COM

Altera's portfolio of FPGAs, structured ASICs, and CPLD products targets many traditional electronics markets. Building on the Stratix device family, the new 65-nm Stratix III FPGAs incorporate features, including dedicated DSP blocks, to combine high performance with the lowest possible static- and dynamic-power consumption; these new devices deliver as much as 50% better power performance than the previous-generation high-end FPGA devices. Stratix III FPGA features include Programmable Power Technology, selectable core voltage, process and circuit technologies, and support from the Quartus II PowerPlay power-analysis and -optimization technology. Stratix II GX FPGAs with transceivers feature superior signal integrity and jitter performance, along with the ability to support optimal protocol implementations.

Altera's recently announced 65-nm Cyclone III FPGAs with 288 embedded multipliers for DSP applications target high-volume applications requiring low power, high performance, and low cost. Hard-Copy II devices give volume-driven-application designers the ability to seamlessly migrate their designs from high-end Stratix series FPGAs to low-cost structured ASICs. The company offers a library of IP (intellectual-property) cores, including the Nios II embedded processor. The Quartus II design software supports all Altera products for FPGA, structured- ASIC, and CPLD designs.

AMI SEMICONDUCTOR, WWW.AMIS.COM

AMI Semiconductor supplies integrated mixed-signal and structured-digital products that target the automotive, medical, industrial, communications, and military/aerospace markets in North America, Europe, and the Asia Pacific region. The company's BelaSigna product family supports high-fidelity, programmable, and ultralow-power systems for portable-audio applications. The company offers a new, miniaturized version of the BelaSigna 200 audio-processing chip that targets small-form-factor, precision-audio products for the consumer and industrial markets.

Innovations for the BelaSigna 200 and BelaSigna 250 DSP-based audio-processing systems include an echo-cancellation algorithm that provides high-quality, echo-free communication in office-telecom headsets and Bluetooth mono and stereo headsets. The company also introduced an acoustic-shock algorithm to mitigate the problems of acoustic shock in products such as communication headsets. The hardware/software combination allows manufacturers to design products that protect users from injury and help employers conform to workplace-safety legislation. The AMIS RPM (Rapid Prototyping Module), featuring the BelaSigna 250 audio processor, enables audio-device developers to evaluate the DSP and subsystems.

ANALOG DEVICES, WWW.ANALOG.COM

Analog Devices' DSP offerings include the Blackfin, SHARC, and TigerSHARC families of processors. Development tools for all of the company's processors include VisualDSP++, VisualAudio, and Ez-Kit Lite, as well as tools from SigmaStudio, uClinux, and Green Hills Software. The Blackfin processor family combines a 32-bit RISC-like instruction set with 16-bit dual MAC (multiply/accumulate) units and targets convergent applications with audio-, video-, and data-processing requirements. The devices' dynamic power management enables lower power consumption by supporting the simultaneous adjustment of system operating frequency and voltage under application control.

The new Blackfin ADSP-BF54x family features increased I/O and memory bandwidth; increased on-chip memory; and the integration of high-bandwidth multimedia peripherals, including a 24-bit LCD. The BF54x family also supports CAN (controller-area-network) and MOST (media-oriented-systems-transport) system peripherals for industrial and multimedia/networked in-vehicle-automotive applications, and it embeds new Lockbox secure technology to protect designers' intellectual property: The Blackfin ADSP-BF52x family targets portable applications, including PMPs (portable media players), VOIP (voice-over-Internet Protocol) phones, IP (Internet Protocol) cameras, and mobile TV. The Blackfin family requires as little as 0.16-mW/MHz core power at 250 MHz, and it incorporates Lockbox secure technology for implementing DRM (digital-rights-management)-content protection.

The SHARC processor family targets applications ranging from consumer, automotive, and professional audio to industrial, test and measurement, and medical equipment. Based on a 32-bit floating/fixed-point core architecture, SHARC-family processors implement a sophisticated memory- and I/O-processing subsystem.

The TigerSHARC processor family offers high floating- and fixed-point performance. It supports glueless-multiprocessor scalability targeting wireless-communications-infrastructure, medical- and industrial-imaging, and military applications.

Analog Devices also offers a line of precision analog microcontrollers with ARM7 or 8052 cores that integrate analog components, such as converters, voltage references, and temperature sensors with the processor core and embedded flash memory. New to the portfolio are

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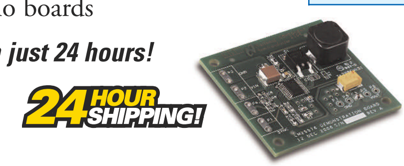

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LM25576	6 to 42	3	TSSOP-20-EP
LM5575	6 to 75	1.5	TSSOP-16-EP
LM25575	6 to 42	1.5	TSSOP-16-EP
LM5574	6 to 75	0.5	TSSOP-16
LM25574	6 to 42	0.5	TSSOP-16

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the ADuC703x family of precision battery monitors for automotive applications and the ADuC7128 precision analog microcontroller for motor-control and smart-sensing applications in industrial- and automotive-system designs.

Analog Devices SigmaDSP audio processors provide a single-chip audio system with a 28/56-bit audio DSP, ADC, DACs, and microcontrollerlike control interfaces. Signal-processing elements include equalization, crossover, bass enhancement, multiband-dynamics processing, delay compensation, speaker compensation, and stereo-image widening. You can use this feature to compensate for the real-world limitations of speakers, amplifiers, and listening environments.

ARC INTERNATIONAL, WWW.ARC.COM

ARC International licenses configurable media subsystems as well as ARC 600 and ARCCPU/DSP cores that enable SOC (system-on-chip) designers to target a range of embedded-system applications. ARC has nearly 140 customers that collectively ship almost 200 million ARC-based units per year to high-growth markets, such as consumer electronics, wireless communications, voice/data networking, and storage.

The ARC 600 ultralow-power cores implement a five-stage pipeline, and the family of cores targets battery-operated and cost-sensitive consumer, networking, and automotive applications. The ARC 700 high-performance cores implement a seven-stage pipeline, which targets computationally intensive graphic, media-codec, and packet-processing applications. The ARC 700 cores support high-end embedded operating systems.

ARM, WWW.ARM.COM

The ARM OptimoDE data-engine licensable IP (intellectual property) has an associated tool environment that combines the efficiency of fixed logic with the benefits of software programmability. Designers can optimize the data-engine architecture to support classes of applications; for example, the AudioDE is tuned for digital-audio processing. Designers can program the architecture to support multiple algorithms with similar requirements using the same data-engine hardware. The devices can accommodate incremental design changes or alternative algorithms with software changes without altering the underlying hardware architecture.

ATMEL, WWW.ATMEL.COM

Atmel bases its DSC (digital-signal-controller) families on its new AVR32 UC3 core, its AVR32 AP7 core, and ARM's ARM926EJ-S core, as well as on a family of dual-core VLIW (very-long-instruction-word) floating-point DSPs that it bases on its mAgic core. The AP7000 DSCs implement a seven-stage pipeline that supports out-of-order execution and SIMD (single-instruction-multiple-data) instructions. Atmel's ARM9-, AVR32 AP7-, and AVR32 UC3-based DSCs implement the same peripheral set, which includes DMA on all peripherals, Atmel's peripheral DMA controller, a multilayer high-speed-bus architecture, an Ethernet MAC (media-access controller), a USB host/device, an ADC, serial-communication peripherals, and an optional external bus interface.

The new UC3 Series A family of 32-bit flash DSCs delivers 80 DMIPS (Dhrystone millions of instructions/sec) at 66 MHz and consumes 40 mA. It has 220 freely intermixable 16- and 32-bit extended instructions that include single-cycle MAC operations, multipliers, atomic memory manipulation, and load/store instructions with on-the-fly data manipulations, such as load-and-insert bit fields, load and swap, and store and swap. The three-stage pipeline integrates single-cycle read/write SRAM with a direct interface to the CPU or AHB (Advanced Microcontroller Bus Architecture high-speed bus). The execution stage's three subunits are an ALU, a multiplication unit, and a load/store unit. UC3 Series A DSCs have 256 to 512 kbytes of on-chip, dual-bank flash that can output one word every clock cycle with or without a wait state.

CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGE CONSULTANTS.COM

Cambridge Consultants' expertise ranges from semiconductors, wireless communications, radar systems, advanced sensors, and control systems in automotive electronics, medical devices, and consumer goods. The company has extensive IC-design capabilities, particularly in high-precision analog-, mixed-signal, and RF systems.

The company's portfolio of IP (intellectual-property) and development tools includes a library of analog, digital, mixed-signal, and wireless IP cores along with embedded-software-development and debugging tools, protocol stacks, and design platforms for ASICs and FPGAs. The IP cores are portable and flexible, and designers can tailor them to their specifications with flexible licensing contracts that can be royalty-free. Cambridge Consultants' silicon-IP offering includes 16- and 32-bit XAP processor cores and the APE2 configurable-data-path DSP.

CEVA, WWW.CEVA-DSP.COM

Ceva shipped more than 190 million customer chip sets in 2006 with Ceva IP (intellectual property), a 45% increase over units shipped in 2005. Last year, Ceva introduced the Ceva-X1622 DSP core and the Ceva-XS1102 system platform. Ceva also introduced the Ceva-X1641 as the first Quad-MAC (multiply-accumulate)-unit DSP core in the scalable Ceva-X family, which executes highly computationally intensive tasks that require substantial data throughput and high memory bandwidth.

Ceva continues to offer products it bases on the Ceva-TeakLite-II DSP core. The low-power, low-cost, programmable Xpert-TeakLite-II DSP subsystem targets 2/2.5G-wireless, portable-multimedia-player, consumer- and professional-audio, VOIP (voice-over-Internet Protocol), VO-Cable (voice-over-cable), VODSL (voice-over-digital-subscriber-line), and VOFTTH (voice-over-fiber-to-the-home) applications. The Ceva-VOP (voice-over-packet) platform targets cost-sensitive residential and consumer VOIP products. The Ceva-Audio fully synthesizable soft IP targets high-performance, low-power audio applications, such as portable audio players, cellular handsets, and home-entertainment systems. Ceva implements its Mobile-Media2000 platform, which it based on the Ceva-X1620 DSP, on a 130-nm process from United Microelectronics Corp with operating speeds that exceed 400 MHz.

Ceva also offers the Ceva-X-, Ceva-X1620-, Ceva-XS1100-, and Ceva-XS1200-based DSP cores and platforms

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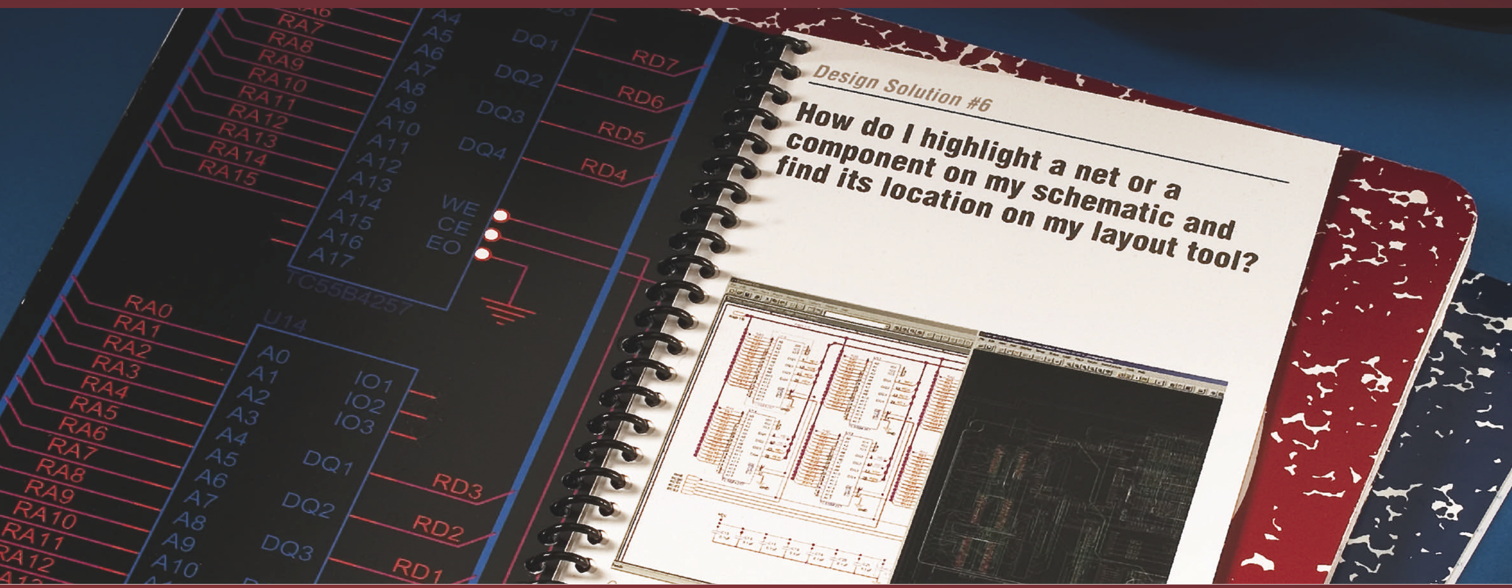

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for licensing. The multipurpose Ceva-X architecture enables multiple derivative cores targeting 2.5/3G multimedia phones, PDAs, digital cameras and camcorders, DTVs (digital televisions), set-top boxes, and HD-DVD. The Ceva-X1620 is the first implementation of the Ceva-X architecture family. The low-power Ceva-XS1100 SOC (system-on-chip) platform targets 3G wireless-baseband designs. The low-power Ceva-XS1200 SOC platform targets high-performance applications, such as multimedia, communications, VOIP, and storage.

CHIPWRIGHTS, WWW.CHIPWRIGHTS.COM

ChipWrights did not provide an update to this year's directory. The fabless-semiconductor company offers video-processing technology to reproduce lifelike imagery in mobile personal-entertainment products, digital-video/digital-still "dual cams," and high-demand video applications, such as security cameras and digital television. The CW5521 SIMD (single-instruction-multiple-data) processor combines a RISC processor; a parallel processor with 16 32-bit datapaths; enhanced video-sensor features; and USB, audio-codec-compact-flash, and secure-digital-card interfaces.

CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic offers DSPs for audio applications. The company's portfolio includes single-core and multicore DSPs for consumer markets, as well as CobraNet audio-system processors for professional, commercial, and consumer markets. These devices feature the vendor's CobraNet technology for delivering uncompressed digital audio over Ethernet networks. The company offers a comprehensive library of audio algorithms, including THX Ultra2, DTS ES (digital-theater-system extended surround) 96/24, Dolby Surround Pro Logic IIx, and a modular programming environment for easy customization. The framework includes state-of-the-art decoders, virtualizers, surround simulators, and audio-enhancement algorithms.

Cirrus Logic this year introduced the CS48520/40 DTV (digital-television) audio processors, which offer a set of audio features and improved performance for DTV applications. To assist in the programming of this and other 32-bit audio DSPs, the company released a graphical programming tool that enables quick custom programmability of the basic audio parameters.

CLARKSPUR DESIGN, WWW.CLARKSPUR.COM

Clarkspur Design did not provide an update to this year's directory. The company offers 16-, 24-, and 32-bit DSPs. Clarkspur's emulator boards support USB-cable controls, and the company offers license-free audio-compression programs, such as OggVorbis.

CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Cradle Technologies is a fabless-semiconductor company that develops multicore DSPs targeting next-generation multimedia applications. Cradle delivers high-performance scalable DSP-programmable platforms for video and imaging in security and surveillance, high-performance imaging, and broadcast and IPTV (Internet-Protocol-television) infrastructure applications. The CT3616, Cradle's flagship multicore system, can provide real-time encoding of Main Profile H.264 at standard-definition resolution on one chip.

Cradle's new Janus PCI DVR, a production-ready, low-cost reference design, features the high-performance CT3616. Janus distinguishes itself in the surveillance-DVR market with the ability to simultaneously encode as many as 16 channels of video and audio using a single CT3616 multirate DSP and also reserves headroom for intelligent video-content-analysis applications or playback.

Cradle recently released the latest version of its multicore-development tools. The software-tool suite comprises Cradle's Eclipse-based IDE (integrated development environment), supporting project-management automation and code development in C, C++, and C-like assembly; the Inspector graphical-debugging environment; the graphical runtime-analysis multicore-profiling tool; and an extensive library of modules for video, image, and I/O processing.

EVATRONIX, WWW.EVATRONIX.PL

Evatronix offers IP (intellectual-property) cores and electronic-design services, including a range of processor, USB, serial-interface-controller, data-communication, and networking cores. The company offers two families of programmable DSP cores. The 16-bit C32025 family targets industrial, home, and consumer applications, and the 24-bit C56000 core targets more complex and accurate applications, such as audio compression and image processing.

FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

Freescale Semiconductor offers programmable DSPs that target audio, mobile-handset devices, and advanced communications-infrastructure equipment. The company's MXC architecture separates the two primary domains of a cell phone into a modem core that communicates with the base station and an application core that drives the user interface. The MXC family includes platforms targeting 2.75G and 3G mobile applications. The Symphony family of DSPs targets high-fidelity professional-, consumer-, and automotive-audio applications. Freescale continued to enhance and expand its 16-bit DSC (digital-signal-controller) portfolio, which it built on its flagship 56F8000 DSC family.

Last year, Freescale introduced the quad-core MSC8144, which it based on the SC3400 third-generation StarCore architecture.

HYPERSTONE, WWW.HYPERSTONE.COM

Hyperstone's E1-16XSR/32XSR RISC/DSPs provide seamless, integrated RISC/DSP functions for applications requiring a high-speed microprocessor and a high-performance DSP. These processors feature dual RISC/DSP execution units in a pipelined architecture sharing the same registers. Designers can freely mix RISC- and DSP-specific programming. To support high throughput, the system executes the RISC/DSP instructions with a high degree of parallelism. These processors target telephony, VOIP (voice-over-Internet Protocol) telephony, video,

digital cameras, and general signal-processing applications.

Hyperstone built the HyNet series of HyNet32XS/32S networking processors around the E1-32XSR core. The company then added integrated peripherals supporting Ethernet, real-time-Ethernet, serial, and ATM (asynchronous-transfer-mode) communications; additional internal RAM; video interfacing; PCI support; and DMA. These processors target industrial and wired/wireless-communication applications that require high-speed signal processing, communications, or both, including real-time Ethernet.

Hyperstone's new E2 RISC/DSP incorporates the E1-32XSR RISC/DSP 0.18-micron core with a high-speed serial-communication engine, 32 kbytes of internal SRAM, an SDRAM interface, a multiplexed-input ADC, and interrupt and DMA controllers. This processor is low- cost and highly integrated for cost-sensitive applications. Its target applications are audio, consumer, and general-purpose signal processing. Hyperstone also introduced a development-tool set for its processor line, basing it on the Eclipse IDE (integrated development environment), including the GNU tool set.

IMPROV SYSTEMS, WWW.IMPROVSYS.COM

Improv offers the Jazz PSA (Programmable System Architecture) platform, which is a configurable, multiprocessor architecture. Rather than use a fixed processor and instruction set, designers can create their own application-optimized processor cores for their products or application domains. Improv's Jazz Processor VLIW (very-long-instruction-word) architecture provides high performance through parallel execution of operations, targeting computationally intensive applications, such as media processing, digital-signal processing, and communication applications. The Jazz DSP cores are also general-purpose, fixed-point DSP cores for general DSP programming.

The Jazz PSA standard tool suite provides a robust and complete development environment for creating optimized DSP software. Central to this environment is the Jazz PSA compiler, targeting VLIW and DSP optimization. The Jazz PSA standard tool suite is retargetable to any configuration of the Jazz PSA platform. The Jazz PSA composer tool suite, a graphical environment for creating designer-defined DSP cores, enables designers to create these configurations.

Improv offers preconfigured cores that are complete hardware and software implementations for high-growth emerging markets. Jazz Media cores include video-, audio-, image-, and speech-processing implementations targeting consumer-electronics devices ranging from mobile handsets to portable media players to high-definition digital displays. Jazz Voice cores address the needs of the voice-over-packet market, including all points of the voice network.

INFINEON TECHNOLOGIES, WWW.INFINEON.COM

Infineon Technologies offers families of 8-, 16-, and 32-bit microcontrollers, with each family offering digital-signal-processing capabilities. The 8-bit XC800 family offers the on-chip Vector Computer, which is a set of coprocessors that includes a hard CORDIC (coordinate-rotation-digital-computer) module for trigonometric/rotational calculations. The CORDIC module supports Park transforms, angle calculation, and determination of multiply accumulates. The Vector Computer includes an MDU (multiply-divide unit), which performs 16- and 32-bit math independently of the 8051 core. With the CapCom6E (enhanced PWM) and fast ADC, these peripherals redefine the capabilities of an 8-bit controller for motor-control schemes, such as for sensorless field-oriented control.

The 16-bit XC16x family of digital-signal microcontrollers contains a MAC (multiply-accumulate) unit and receives support from a functional DSP library available online from Infineon. The XC16x family is available with onboard flash ranging from 32 to 256 kbytes. It has the same CapCom6E unit as the 8-bit XC800 family, which the ADC may trigger independently of the CPU. These devices target motor-control schemes such as constant-VF, frequency slip, and field-oriented control.

Infineon bases the TC116X family of 32-bit microcontrollers on the TriCore unified-microcomputer/DSP architecture, which operates as a single multitasking engine with fast context switching. Target applications include servo control, audio-domain digital-signal processing, data communications, modems, automotive systems, and portable systems.

IPFLEX, WWW.IPFLEX.COM/EN

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting imaging and video, communication/wired, medical, and automotive applications. The company's DAPDNA (digital-application-processor/distributed-network-architecture) incorporates a RISC processor as a controller with a heterogeneous matrix of 300 to 1000 processing elements. The DNA architecture can reconfigure within one clock cycle to deliver to designers flexible, field-programmable, and high-performance processing. IPFlex offers the DAPDNA-2 and DAPDNA-IMS product lines. DAPDNA-IMS products target imaging and video applications, and DAPDNA-2 products target multiple purposes for various applications.

IPFlex offers tools and evaluation boards for developing DAPDNA-based high-performance systems. The DAPDNA-FW II design tools include a Data Flow C compiler that enables developers to describe their algorithms in a C-like syntax, which is partly based on Handel-C, and automatically generates hardware code. IPFlex also offers application IP (intellectual property) to optimize the performance of DAPDNA and assist designers with their end applications.

LATTICE SEMICONDUCTOR, WWW.LATTICESEMI.COM

Last year, Lattice Semiconductor introduced two second-generation families of low-cost, 90-nm FPGAs that include dedicated DSP blocks. These families, the LatticeECP2 and LatticeECP2M devices, include hard-DSP blocks that designers can program to implement functions such as multiply, multiply-accumulate, and multiply-add/subtract. The families provide as many as 100,000 LUTs (look-up tables), 168 18×18 multipliers, 5.3 Mbits of block memory, and 16 channels of 3.125-Gbps SERDES (serializer/deserializer). These low-cost FPGAs provide both DSP and SERDES functions.

Lattice also released a number of IP

(intellectual-property) cores that allow the implementation of DSP functions within the LatticeECP2 and LatticeECP2M devices. They support functions including FFT (fast-Fourier-transform) compilers, FIR (finite-impulse-response)-filter generators, Reed-Solomon encoders and decoders, convolution encoders, Viterbi decoders, and turbo-coding functions. The Lattice IPexpress tool includes all of these IP cores, allowing users to parameterize and generate IP on their desktops. The IPexpress tool also allows the trial use of IP cores in the design before purchase. Lattice's ispLever suite of design tools includes the IPexpress tool.

LSI LOGIC, WWW.LSILOGIC.COM

The LSI Zevio 1020 application processor from LSI Logic targets electronic toys, navigation systems, portable media players, and other mobile products. The chip integrates an ARM9 processor for general-purpose processing; a DSP for multimedia processing, such as H.264 video decoding; a 3-D-graphics processor for enriched content development; and a 2-D/3-D sound processor for MIDI playback and 3-D sound effects. It also integrates video-DAC for direct TV- or LCD-screen output, and an SDIO (secure-digital-input/output) card slot for data storage or peripheral expansion.

The Zevio 1020 uses a multiprocessor architecture that provides the flexibility to use dedicated processors optimized for a variety of tasks. The Zevio 1020 consumes less than 200 mW for 3-D-graphics processing and H.264 video decoding. By distributing the tasks among multiple processors that run at optimal frequencies, the Zevio 1020 optimizes cost, power, and performance. LSI supports custom-SOC (system-on-chip) developments based on the Zevio architecture with a menu of preverified IP (intellectual-property) blocks.

MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM/DSPIC

Microchip's 16-bit (data) dsPIC DSC (digital-signal-controller) modified-Harvard-RISC machine combines the control advantages of a high-performance, 16-bit microcontroller with the high computational speed of a fully implemented DSP to produce a tightly coupled, single-chip, single-instruction-stream implementation for embedded-system design. All of Microchip's 16-bit DSC and microcontroller families share the same core instructions (with the DSCs adding DSP instructions to the set), peripherals, and development tools and have compatible pinouts. Microchip released five more devices in the dsPIC30F family, along with 19 members of the newer dsPIC33F family. The cumulative total of dsPIC DSCs in production stands at 43. The dsPIC33F family is growing, with flash memory ranging from 12 to 256 kbytes and pin counts of 18 to 100, in a number of peripheral configurations.

The standout products this year were the dsPIC30F1010/2020/2023 family for SMPSs (switched-mode power supplies) and digital-power conversion, which couples a flexible DSC core with peripherals for the task. The devices' digital PWM, ADC, and analog-comparator modules tie together to form an Intelligent Power Peripheral. The digital PWM provides 1-nsec resolution over seven PWM modes. This configuration is essential for SMPS applications and enables a broader range of applications, including isolated dc/dc converters, power-factor correction, uninterruptible power supplies, and digital lighting. The onboard 2M-sample/sec ADC can be precisely timed. The onboard analog comparators can terminate the PWM pulse early for "cycle-by-cycle current limiting"—a key feature for current-mode and next-generation power supplies. Finally, the DSCs are available in packages with 28 to 44 pins and as small as 6×6 mm, including the internal flash memory and including the peripherals necessary for single-chip operation.

A new feature Microchip introduced for all dsPIC DSCs is CodeGuard secure-segmented-memory protection, which allows multiple parties in a collaborative-system design to share the memory, interrupts, and peripherals of one chip, without compromising their IP (intellectual property). This memory segmentation reduces system costs for OEMs and their design partners by eliminating the need to store programs on separate chips. These features enable code protection in a secure-memory segment, separate from upstream code, that tailors the code to an application. Alternatively, you can use

CodeGuard security for secure firmware updates.

MIPS, WWW.MIPS.COM

MIPS Technologies offers embedded-processor architectures and cores targeting digital-consumer, networking, personal-entertainment, communications, and business applications. The company licenses its 32- and 64-bit RISC-IP (intellectual-property) architectures and 32-bit processor cores to semiconductor companies, ASIC developers, and system OEMs. Industry-standard tools, software, and services support the MIPS architecture; more than 120 companies have licensed MIPS IP processors for inclusion in their SOC (system-on-chip) designs.

The MIPS32 24KE and MIPS32 34K core families feature DSP extensions for improved signal-processing performance. The 34K cores are the first to integrate the MIPS MT (multithreaded) ASE (application-specific extension). The architecture improves processing throughput by feeding additional threads into the pipeline as one thread stalls for memory accesses or for other shorter-term pipeline stalls.

MORPHO TECHNOLOGIES, WWW.MORPHOTECH.COM

Morpho Technologies did not provide an update to this year's directory. The company focuses on processing engines for software-defined radio. Morpho Technologies offers MS2, a platform for ultralow-power software-multimode radio, targeting applications such as handsets. In addition, Morpho licenses a WiMax (worldwide-interoperability-for-microwave-access)-system product through integrated hardware and software IP (intellectual property), and it includes the MS2 PHY (physical-layer) communications engine.

NXP SEMICONDUCTORS, WWW.NXP.COM

Last year, Philips spun off its semiconductor business to form NXP Semiconductors. The new company retained ownership of the Nexperia family of media processors, which targets connected multimedia products in the mobile wireless, audio, imaging and video, and consumer markets. Forming the DSP component of the Nexperia brand is NXP's Adelante technology, which includes the classic 16-bit RD1602x and 24-bit RD2412x DSP cores with a user-definable VLIW (very-long-instruction-word) architecture. The high-performance Adelante VD3204x Embedded Vector DSP family rounds out NXP's offering. With its innovative vector-processing architecture, which minimizes power consumption, the VD3204x targets highly computationally intensive functions in communication and broadcast-reception applications. Adelante provides its DSP technology with the Adelante software-development kit, a verification environment for multicore SOC (system-on-chip) architectures.

ON DEMAND MICROELECTRONICS, WWW.ODM.AT

ODM (On Demand Microelectroncs) offers IP (intellectual property) and SOCs (systems on chips) targeting the upcoming global digital-video revolution. The basis for ODM's product portfolio is the silicon-proven VSP (vector-signal processor)—a scalable, configurable, and fully software-programmable processor. The VSP is most suitable for handling applications of DSP with extremely high-performance demands, such as digital video. One of the primary IP cores the ODM offers is SVEN (Scalable Video Engine). SVEN can handle high-definition, multistandard-compliant video-codec implementations for resolutions as high as 1080i/720p. Supporting SVEN, ODM offers Pictor, a high-end image-processing platform, and Samba, the first IP for multistandard baseband processing on the market. The latest implementation is SVENm, a 90-nm multimedia chip targeting mobile applications.

PICOCHIP, WWW.PICOCHIP.COM

PicoChip did not provide an update to this year's directory. The company offers multicore-signal-processing products targeting wireless systems and software-defined-radio designs. The company offers a family of processors having 200G-instructions/sec and 40-GMAC (giga-multiply-accumulate)-operation performance with a suite of software-development tools and reference designs. The picoArray is easy to program in a standard, familiar development environ-

ment. The company supplies standards-compliant protocol stacks and software-certified, upgradable reference designs for the WCDMA/HSDPA (wideband-code-division-multiple-access/high-speed-downlink-packet-access) and WiMax/WiBro (worldwide-interoperability-for-microwave-access/wireless-broadband) protocols. The company's PC102 processor is available in volume production.

PIXELWORKS, WWW.PIXELWORKS.COM

Pixelworks did not provide an update to this year's directory. The company designs, develops, and markets semiconductors and software for the advanced- display industry, including advanced TVs, multimedia projectors, digital-streaming-media devices, and LCD panels. Pixelworks' line of programmable BSPs (broadband-signal processors) can handle multiple codecs for high-quality IPTV (Internet Protocol-TV) video and other digital-video applications. The company offers the DreamStream application-reference software for designers using the BSP chips. Pixelworks also offers devices ranging from single-purpose discrete ICs to SOCs that can process and enhance the video signal throughout the entire path in the system.

PHILIPS SEMICONDUCTORS

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas Technology's SuperH family includes a series of high-performance 32-bit RISC processors with DSP capabilities. The SH-2A and SH-4A employ a superscalar architecture with a built-in FPU (floating-point unit) for higher performance, delivering as much as 1080 MIPS. The SuperH architecture integrates both DSP and FPU capabilities into a single RISC CPU core to save power and overall system cost. These devices are compatible with the previous-generation devices. Development tools, operating systems, on-chip debugging controllers, emulators, and other tools from third parties support all SuperH processors.

Last year, Renesas introduced three new groups of SH-2A series microcontrollers with an FPU capability. The SH7211F supports an operating speed of 160 MHz and 512-kbyte flash memory, targeting office-automation and consumer products. The SH7263 offers 480 MIPS performance at 200 MHz. Its built-in USB-host interface enables seamless connectivity to digital-audio players and an integrated LCD controller for QVGA-size color screens. The SH7652, which operates at 200 MHz, is the first device to incorporate both a copyright-protection function for IP (Internet Protocol) broadcasting and the DTCP (Digital Transmission Content Protection)-IP standard for high-definition DTVs (digital TVs).

For high-end multimedia, Renesas rolled out two new groups of microprocessors that use the top-end SH-4A CPU core. The SH7764 multimedia processor incorporates a 2-D-graphics engine, an Ethernet controller, a USB-host/function controller, an ATAPI hard-drive controller, and an LCD controller. The SH-MobileR addresses a multimedia need beyond mobile phones, delivering a video- and DTV-enabled technology to car-navigation systems, portable media players, and VOIP (voice-over-IP) video phones.

RC MODULE, WWW.MODULE.RU

The RC (Research Center) RISC/DSP-architecture design center provides silicon IP (intellectual property) for VLIW/SIMD (very-long-instruction-word/single-instruction-multiple-data) processors with a flexible and high-performance, 1- to 64-bit vector-matrix engine. RC Module offers mixed-signal SOC (system-on-chip) design service and application-software development for industrial radio-navigation, consumer standard- and high-definition TV, and other math-intensive applications. Software- and hardware-development tools, as well as real-time signal- and video-image-processing systems are available from RC Module. The company develops smart devices for intelligent-transport systems, such as the TrafficMonitor, a real-time traffic-data-collection and -analysis video system.

This year, RC Module presents the new NeuroMatrix NM6404, a 0.25-micron, high-performance DSP targeting real-time data-flow processing. The company based the processor, which includes 2 Mbits of on-chip memory, on the advanced VLIW/SIMD NMC2 core. It also supports new software-development tools for the NeuroMatrix DSP family. The NMServer software provides service access to the boards with NM640x processors from a remote PC.

RF ENGINES, WWW.RFENGINES.COM

RF Engines did not provide an update to this year's directory. The company's cores and SOC (system-on-chip) designs primarily target Xilinx and Altera FPGAs for applications in wireless-communications systems, electronic warfare, spectrum analysis, and medical instrumentation. The standard range of cores includes the HyperSpeed cores for applications requiring 6.4G-sample/sec performance. The HyperLength cores support a 1 million-point transform running at complex sample rates as high as 200M samples/sec on a Xilinx Virtex-II 3000. The Matrix cores include a set of different-length DFT (discrete-Fourier-transform) cores that combine to allow the configuration of an FFT (fast Fourier transform) to match the number of points an application requires.

The ChannelCore64 can extract as many as 64 narrowband channels from one or two wideband ADC inputs. The PFT (pipelined-frequency transform) multichannel-filter bank targets use in real-time applications. The Polyphase DFT, or WOLA (weighted overlap and add), is a method of implementing a uniformly distributed multichannel-filter bank. The tunable PFT supports on-the-fly reconfiguration to any frequency plan as a digital front end for the telecommunications, defense, and instrumentation markets. The SpectraChip cores provide a digital replacement for analog intermediate-frequency filtering; the digital implementation includes standard features, such as resolution-bandwidth filtering, video-bandwidth filtering, and conversion to log power.

SENSORY, WWW.SENSORYINC.COM

Sensory did not provide an update to this year's directory. The company's RSC family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line supports speaker-independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, 2400-bps speech compression for speech playback, and music synthesis.

The RSC-4x family provides on-chip feature integration, including a microphone preamplifier, twin-DMA units, a vector accelerator, and a hardware multiplier that allows you to build a system with little more than a battery, a speaker, a microphone, and a few resistors and capacitors. Multiple ROM options are available.

Sensory's SC-6x series of DSPs offer multiple options for introducing speech- and music-synthesis abilities into consumer products. Members of the SC-6x line can store as much as 37 minutes of speech on-chip and include as many as 64 I/O pins for external interfacing.

SILICON HIVE, WWW.SILICONHIVE.COM

Semiconductor-IP (intellectual-property) supplier Silicon Hive designs, builds, and licenses application-specific products for communications and media processing, tuned processor cores, and program-development tools with application libraries. Silicon Hive cores target specific application requirements, and they are high-level-programmable from ANSI C.

The company's processor lineup includes the Avispa-CH1, a high-performance, C-programmable data processor for communications-signal processing. The Avispa-IM2 is a general-purpose C-programmable data processor. These processors are scalable to a high level of operations per cycle, with multiple options for precision, I/O, and memory configurations. The C-programmable Moustique-IC2 SIMD (single-instruction-multiple-data) processor targets image-signal processing, with multiple options for SIMD-vector dimension, I/O, and memory configurations. All processors come with a software-development environment, application libraries, and SOC (system-on-chip) integration and verification packages.

STARCORE

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

STMICROELECTRONICS

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

STREAM PROCESSORS, WWW.STREAMPROCESSORS.COM

SPI (Stream Processors Inc) is a fabless-semiconductor company that offers parallel processing to enable demanding signal-processing applications. The company's technology addresses how to make parallel processing easily accessible to programmers. SPI last year began shipping its Storm-1 family of stream processors, targeting video and image processing in applications such as high-definition videoconferencing, intelligent video surveillance, and multifunction printers.

STRETCH, WWW.STRETCHINC.COM

Stretch offers a family of software-configurable processors with embedded programmable logic within the processor to target imaging and video, mobile/wireless, security, and industrial applications. Using familiar C/C++ programming tools, system developers can automatically configure Stretch's processors to flexibly address diverse markets with changing application needs. Stretch's new S6000 family of software-configurable processors targets high-performance video and wireless-signal processing. The S6 architecture offers three technology innovations that include a second-generation ISEF (instruction-set-extension fabric), a processor array, and a programmable accelerator.

Stretch and its partners offer reference hardware and software applications for main-profile standard-definition- and high-definition-resolution MPEG 2 and H.264 video encoding. Many of the core modules from these applications are available in source code as optimized extension instructions. Stretch and its partners also offer hardware and software applications for WiMax (worldwide-interoperability-for-microwave-access) base-station equipment. A number of the physical-layer modules, including FFTs (fast Fourier transforms), FEC (forward-error-correction) functions, and CRC (cyclic-redundancy check), are available in source code as optimized extension instructions.

Stretch enhanced its IDE (integrated development environment) with the Slickedit text-editor tools and improvements in the compiler and instruction-set simulator. A library of code supporting DSP, wireless-signal-processing, and video- and image-processing functions is available.

TENSILICA, WWW.TENSILICA.COM

Tensilica offers several DSP choices within its Diamond Standard processor line. The new Diamond 38xVDO video engines target D1 (standard-definition) resolution and offer H.264 Main Profile encoding, decoding, or both, as well as VC-1/WMV (Windows Media Video)-9, MPEG-4, and MPEG-2 decoding. The Diamond 330HiFi audio processor includes dedicated audio instructions to decrease frequency requirements. Vendors have ported more than 20 popular audio encoders and decoders to the Diamond 330HiFi. The three-issue, VLIW (very-long-instruction-word), eight-MAC (multiply-accumulate)-operation, SIMD (single-instruction-multiple-data) Diamond 545CK is Tensilica's fastest licensable DSP core. Other Diamond Standard processors, including the 212GP and the 570T, incorporate 16-bit MAC operations for easier DSP tasks.

Tensilica's Xtensa processors are configurable, extensible, and synthesizable. Designers can select and configure predefined elements of the architecture and invent instructions and hardware-execution units to maximize performance. Tensilica's Xtensa LX2 processor core with the Vectra DSP engine supports wide datapaths and traditional DSP tasks. The system can deliver RTL-equivalent I/O through a ports-and-queues mechanism that directly connects to the processor's execution unit to bypass the load/store operation. The Vectra LX DSP engine uses 64-bit instruction words containing three-issue slots for ALU (arithmetic-logic-unit), MAC (multiply/accumulate), and load/store operations.

TEXAS INSTRUMENTS, WWW.TI.COM

Texas Instruments offers a broad portfolio of programmable DSPs. The TMS320C6000 DSP platform comprises high-performance fixed- and floating-point DSPs targeting video, imaging, broadband-infrastructure, and performance- audio applications. TI announced the lowest cost TMS320C6720 floating-point DSP for $5.75. It introduced the cost-effective, high-performance TMS320C6454 DSP for infrastructure applications, which is an ideal migration path for current C6416 and C6455 DSP developers.

The TMS320C5000 DSP platform offers low standby power and advanced automatic power management. TI announced the TMS320C5506 DSP that requires only 0.12 mW at 108 MHz in standby mode and 1.2V. TI also introduced the audio-optimized TMS320C54HFK DSP for the Hands Free Kit reference design to allow for differentiating features, including audio streaming and speech recognition.

DaVinci technology consists of scalable, programmable DSP-based SOCs (systems on chips), software, tools, and support for developing digital-video end equipment. The latest processors based on DaVinci technology include the TMS320DM643x processors, priced as low as $9.95 and tuned for automotive vision, video surveillance, and video telephony. TI also recently released the TMS320DM6441 for portable video- and audio-system applications, which require additional power-management features.

The TMS320C2000 DSC (digital-signal-controller) platform combines as much as 150 MIPS of TI's DSP technology with the control-peripheral integration, C-language efficiency, and ease of use of a microcontroller. C2000 DSCs target digital-power supplies, digital motor control, and advanced sensor control in industrial, automotive, medical, and white-goods applications. TI has announced four new hardware- and software-compatible flash and custom ROM-based devices in the C2000 portfolio and four new, low-cost, 32-bit TMS320F280xx devices, offering as much as 60 MHz of performance, with prices starting as low as $3.25 (1000).

TI's new TMS320F28044 controller targets multichannel POL (point-of-load) applications, such as telecommunications and networking-infrastructure equipment, servers, laptops, and industrial equipment. With 100 MIPS of 32-bit DSP performance, the F28044 programmable controller can manage as many as 16 dc/dc-converter channels for multichannel POL applications. The F28044 controller implements as many as 16 channels of TI's patent-pending high-resolution pulse-width-modulation technology, each with 150-psec resolution.

TI also introduced new low-cost digital-power-development kits targeting power-factor correction and dc/dc applications. The kits provide off-the-shelf platforms that work seamlessly with the free DPS (digital-power-supply) software library, which offers reference software for key functions in ac/dc, complex POL, dc/ac inverters, and uninterruptible-power-supply applications.

The single-chip, 3-GHz-performing TMS320TCI6487 wireless-infrastructure baseband processor drives down the cost of GSM (global-system-for-mobile-communications)-based base stations and supports emerging WiMax (worldwide-interoperability-for-microwave-access) and TD-SCDMA applications. Targeting pico to macro base stations, the TCI6487 incorporates three DSP subsystems, each with a 1-GHz, C64x+ DSP core.

3DSP

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

XILINX, WWW.XILINX.COM

Xilinx offers PLDs and FPGAs. The company's XtremeDSP product includes a portfolio of DSP devices that target high-performance signal processing with software tools that support design development in Matlab, Simulink, and C/C++, along with development kits and reference designs in wireless and video applications. XtremeDSP application-optimized products are available for medical-imaging, military/aerospace, mobile/wireless-base-station, imaging, and video systems.

Xilinx DSP devices include the Virtex-4, Virtex-5, and Spartan-3 family of FPGAs that feature as many as 640 18×25 DSP slices capable of operating as fast as 550 MHz. Software tools such as System Generator for DSP and AccelDSP Synthesis suites make it easier for designers who are unfamiliar with FPGAs to port their algorithms. These tools come with a library of parameterizable DSP algorithms, such as FFTs, a filter compiler, FEC (forward-error-correction) algorithms, and video codecs. Xilinx also provides technical support with a dedicated team of DSP field-applications engineers and a hotline.

ELECTRONIC COMPONENTS

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Choose capacitor types to optimize PC sound quality

A KEY CHALLENGE TO DESIGNERS OF AUDIO SUBSYSTEMS THAT MUST CONFORM TO WINDOWS VISTA REQUIREMENTS MAY BE CHOOSING COUPLING CAPACITORS. THESE DEVICES' CAPACITANCE VARIES WITH THE VOLTAGE ACROSS THEM AND INTRODUCES AUDIO DISTORTION. TO MINIMIZE THE EFFECT, START BY UNDERSTANDING THE INTERACTIONS AMONG THE DIELECTRIC MATERIAL, VOLTAGE RATING, DEVICE SIZE, AND VOLTAGE COEFFICIENT. THEN, GET READY TO MAKE TRADE-OFFS.

Microsoft's (www.microsoft.com) next-generation client operating system—now officially known as Windows Vista—is enhancing desktop- and notebook-PC audio quality and fidelity. Hardware manufacturers must meet strict audio-performance requirements to license the Windows Vista logo. Microsoft bases these requirements on audio-performance specifications, such as the THD+N (total harmonic distortion plus noise), dynamic range, and crosstalk. Generally, designers think of audio amplifiers as the limiting factor in performance specifications, such as THD+N. However, passive components in the signal path can introduce THD that contributes significantly to system-level distortion.

Passive components are critical to a successful audio design; they define gain, provide biasing, reject power-supply noise, and establish dc blocking between stages. Unfortunately, portable audio devices' space, height, and cost restrictions force the use of passive components with small footprints, low profiles, and low cost. Failure to understand the nonlinearity associated with these small, low-cost, passive components can affect Vista compliance (**Reference 1**).

Voltage coefficient, temperature coefficient, piezoelectric effect, equivalent-series resistance, equivalent-series inductance, leakage current, dielectric absorption, and tolerance describe how a capacitor's behavior deviates from ideal. The terms most important to understand when you design a signal path for premium audio performance are voltage coefficient and converse piezoelectric effect, which is the main contributor to voltage coefficient.

PIEZOELECTRIC EFFECT

The piezoelectric effect is a property of certain crystals that acquire electrical charges under mechanical loading. The effect originates from the displacement of ionic charges within the crystal structure. Without a mechanical load, the crystal structure is symmetric, and the resulting electric dipole moment is zero. When you apply a mechanical load, the charge distribution is no longer symmetric, and a net polarization results.

The converse piezoelectric effect is the situation in reverse: A change in the applied electric field causes a change of mechanical dimension. Large K-factor capacitors, such as those with Class 2 dielectrics, have a discernible converse piezoelectric effect in which applying an electrical signal causes a change in the capacitor's mechanical dimension. As the applied signal's amplitude increases, the capacitor's physical deformation increases, causing the capacitor's rated electrical value to change. When you place the capacitor at an audio amplifier's input to establish dc blocking between the codec and the amplifier (**Figure 1**), the capacitor's varying electrical value causes a nonlinear, signal-dependent change in the amplifier's transfer function: $T(j\omega)=K/(1-j(\omega_o/\omega))$, where $K=R_F/R_{IN}$ and $\omega_o=1/(R_{IN}C_{IN})$. The circuit's magnitude response, $|T(j\omega)|$, equals $|K|/\sqrt{(1+(\omega_o/\omega)^2)}$. A nonlinear change of capacitor impedance ($1/j\omega C_{IN}$) tends to dominate at low frequencies at which the impedance is significant in defining the gain. This phenomenon translates into audio distortion.

This converse piezoelectric effect is by far the most significant cause of increased distortion at lower audio-band frequencies (**Figure 2**). The effect is maximized at the −3-dB bandwidth, at which the input coupling capacitor's impedance magnitude equals that of the audio amplifier, or $f_{-3dB}=1/(2\pi R_{IN}C_{IN})$. Given the typical values for an audio amplifier's

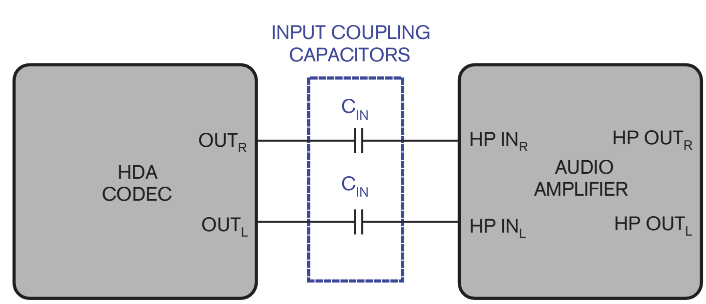


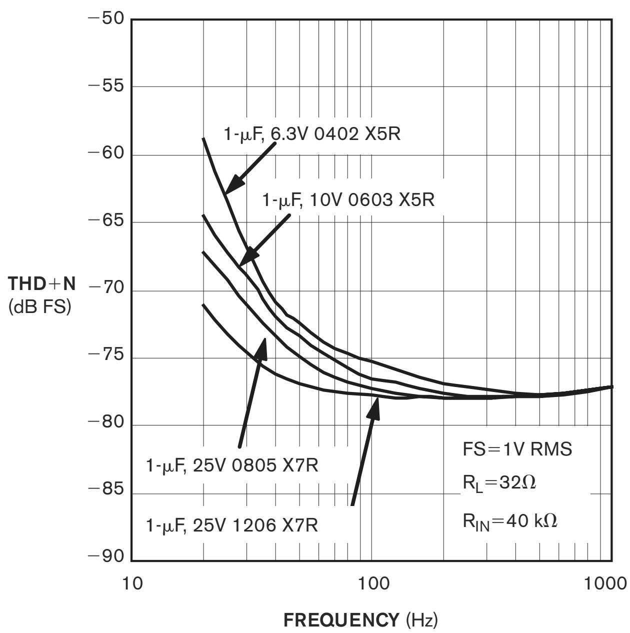
Figure 1 Input coupling capacitors establish dc blocking between the HDA (high-definition-audio) codec and the audio amplifier.

input resistance and input coupling capacitor, −3-dB bandwidth is generally less than or equal to 100 Hz.

In Class 2 low-dielectric capacitors, the converse piezoelectric effect is the major contributor to voltage coefficient—the term that describes how applied voltage affects a component's value. These capacitors react differently depending on whether you apply a changing (ac) voltage or a constant (dc) bias.

Figure 3 illustrates the typical effect of applying dc voltage to various 1-μF capacitors. This dc-voltage value is typical for ac-coupling capacitors at amplifier inputs in PC applications. Applying increasing positive (or negative) dc voltage to Class 2 dielectric materials decreases the capacitor's value. This article does not discuss the mechanics or physics that underlie this phenomenon. Instead, it simply presents measurements of the effect and guides you in selecting capacitor types to optimize PC sound quality.

Although applying increasing dc voltage tends to decrease the capacitance of a Class 2 dielectric, applying an ac voltage



NOTE: FS=FULL-SCALE.

Figure 2 Input-coupling-capacitor-induced total harmonic distortion versus frequency depends on the coupling capacitor's dielectric material, voltage rating, and package size, as well as on the capacitance.

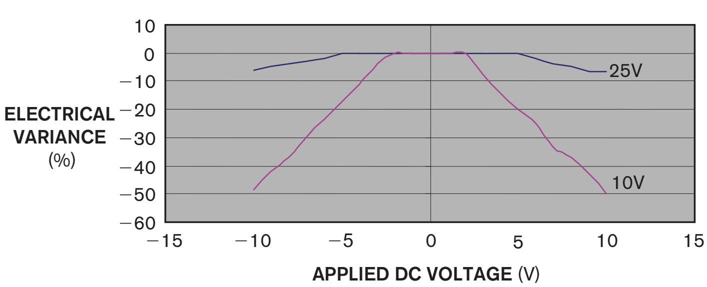


Figure 3 A smaller ceramic capacitor has a lower voltage rating than a larger unit of the same value and dielectric material. Also, a given applied dc voltage affects the smaller device's capacitance more than it does that of the larger unit. You see this effect when you compare the electrical variance with the applied dc voltage of a 1-μF±20%, 25V, X7R, 1206 ceramic capacitor with that of a 1-μF±20%, 10V, X7R, 0603 ceramic capacitor at an ambient temperature of 25°C.

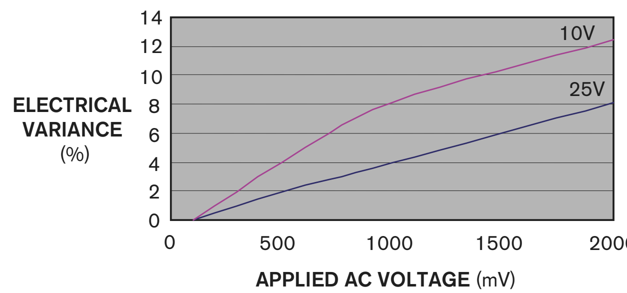
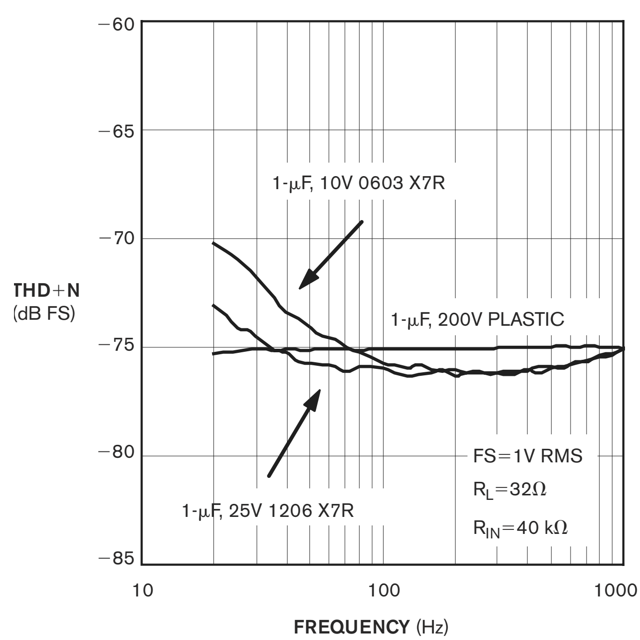


Figure 4 Increasing the amplitude of an ac signal applied to a ceramic capacitor increases the device's capacitance, as you see in these curves. The curves show electrical variance versus applied ac voltage at −3-dB bandwidth of 100 Hz of a 1-μF±20%, 25V, X7R, 1206 ceramic capacitor and a 1-μF±20%, 10V, X7R, 0603 ceramic capacitor at an ambient temperature of 25°C.



NOTE: FS=FULL-SCALE.

Figure 5 The distortion introduced by 10 and 25V, 1-μF X7R ceramic capacitors depends on the audio frequency as well as the capacitor size and voltage rating. You express the effect in terms of THD+N (total harmonic distortion plus noise), although distortion (not noise) dominates this measurement and that of Figure 6.

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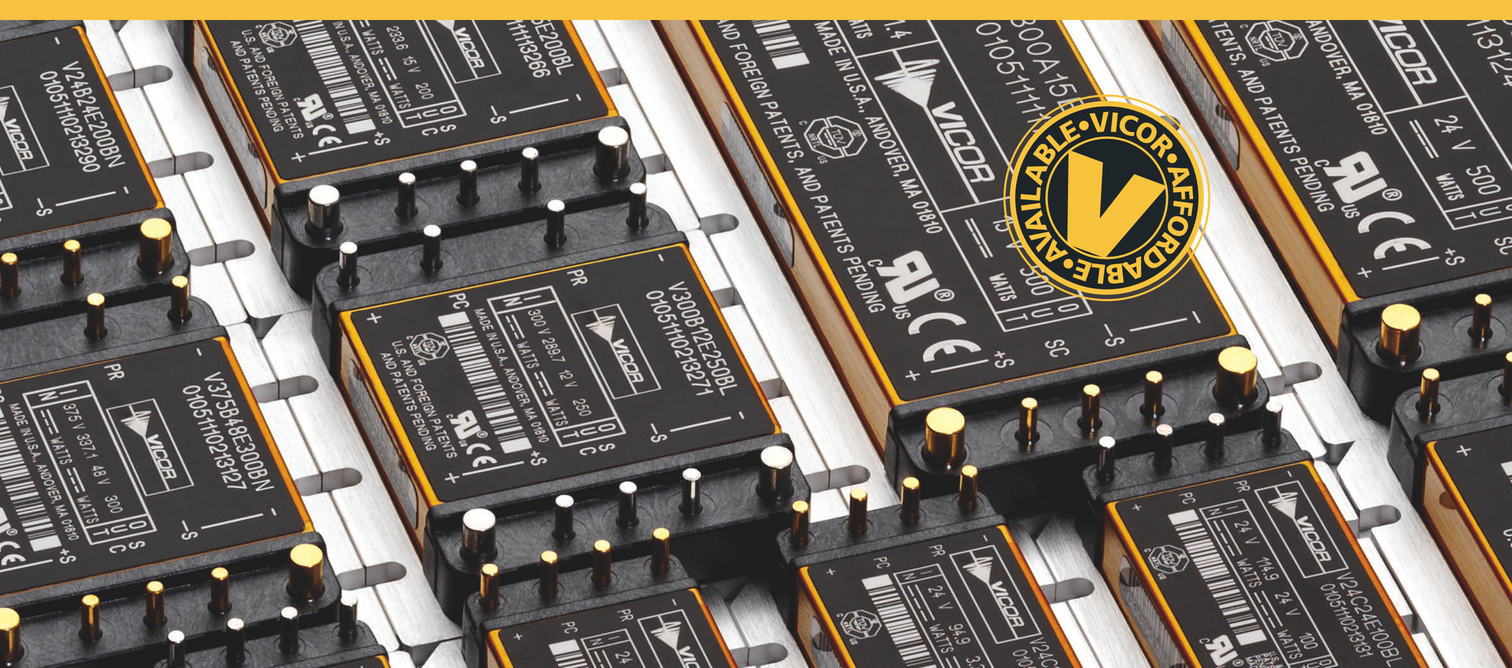


(within a reasonable range) tends to increase the measured capacitance (**Figure 4**). If you apply a high enough ac voltage, the capacitance will eventually decrease in the same manner as it does when you apply dc voltage. However, the high voltage required to cause this effect does not represent the voltage swings you normally find in PC-audio circuits. Therefore, the preceding analysis does not include this voltage level. **Figures 5** and **6** translate into audio performance the effect that **figures 3** and **4** illustrate.

A 1-μF, X7R-dielectric ceramic capacitor resides in series with a Maxim (www.maxim-ic.com) audio-amplifier input whose typical input impedance is 40 kΩ. The device under test varies from 10V-rated (0603 case) to 25V-rated (1206 case) units as a THD+N AP (Audio Precision, http://ap.com) sweep monitors the output distortion at frequencies less than or equal to 1 kHz. Notice the increased distortion when the setup uses the 10V-rated capacitor compared with that using the 25V-rated capacitor.

A low voltage rating (that is, high voltage coefficient) produces greater THD because the capacitor's electrical value varies more during the sinusoidal cycle. To reduce THD in the lower audio-frequency band, you must reduce the voltage coefficient of capacitance. To reduce the voltage coefficient, you should select a capacitor with a higher voltage rating. In Class 2 dielectrics, selecting a higher voltage rating is helpful when attempting to conform to Vista audio specifications. Note, however, that the capacitor's case size increases with the voltage rating. A 1-μF±20% ceramic capacitor with a 10V rating uses an 0603 case size, whereas a 1-μF±20% ceramic capacitor with a 25V rating uses a 1206 case. Regardless of the recent push for ultramobile notebook computers and ever-shrinking PCB (printed-circuit-board) area, headphone-amplifier inputs typically require large-case input-coupling capacitors to achieve Vista compliance for THD+N over the 20-Hz to 20-kHz bandwidth.

DIELECTRIC TYPE

You can regard a capacitor's dielectric type as a potential limitation on premium-THD performance. Various dielectrics affect THD differently. **Figure 7** illustrates the dc-bias depen-

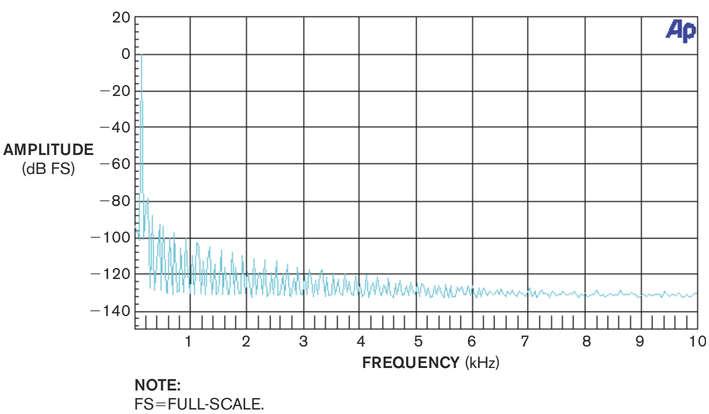


Figure 6 This FFT spectrum analysis also shows the frequency dependence of coupling-capacitor-induced distortion. Full-scale is 1V rms; input frequency is 100 Hz; and the device under test is a 1-μF, 25V, X7R ceramic capacitor (courtesy Audio Precision).

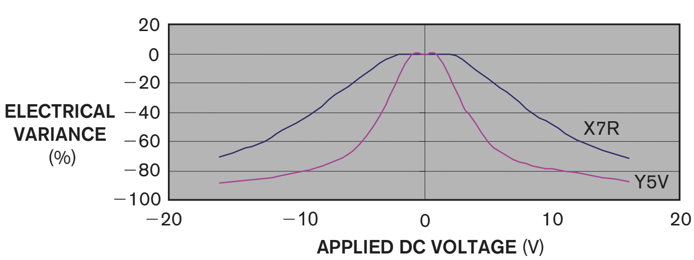


Figure 7 These curves illustrate the dc-bias dependency of two 0603-case-size capacitors with Y5V and X7R dielectrics and equal 16V ratings.

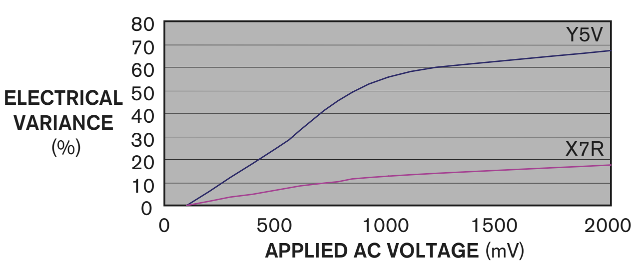


Figure 8 These curves show the variation in capacitance due to applied ac voltage for 16V-rated 0603-case-size capacitors with Y5V and X7R dielectrics.

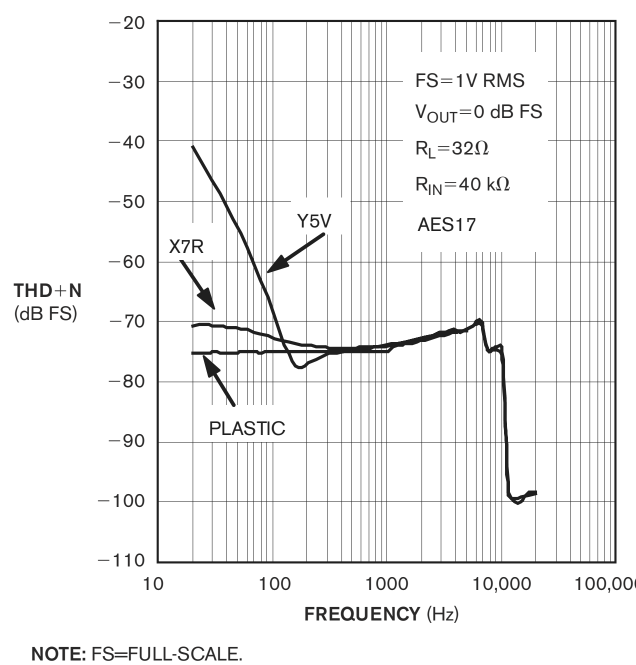


Figure 9 These curves depict the audio distortion that Y5V and X7R, 1-μF±20%, 16V, 0603-cased ceramic capacitors introduce.

MEASURING CAPACITANCE VARIATION

To obtain measurements of its capacitance variation versus applied dc voltage, connect the device under test (C_{DUT}) in series with a 1.5-kΩ±1% resistor (Figure A). C_{DUT} in series with R forms a highpass filter, allowing measurement of the capacitor's electrical value as you increase the applied dc voltage ($C_{DUT}=1/(2\pi Rf_{-3dB})$). Superimpose a 100-mV-rms ac signal on the varying dc-voltage source. Note the highpass filter's −3-dB bandwidth at each 1V-dc increment (Figure B). Vary V dc from 0V to the component's rated voltage.

Note that the resistance of series resistor R must be much greater than the audio analyzer's finite source resistance. In this case, the Audio Precision analog generator presented a 40Ω source resistance.

Also note that a 100-Hz cutoff frequency for this measurement highlights the effects of applied dc voltage above and below the −3-dB bandwidth. A 20-Hz cutoff frequency is not an appropriate choice as the analyzer measures down to only 10 Hz. Vista-Logo Program Requirements V3.09 specifies −3-dB bandwidth at 20 Hz into a 10-kΩ load. Given the −3-dB frequency and the known series-resistor value (1.5 kΩ±1%), you can extract the capacitance of C_{DUT} from Table A.

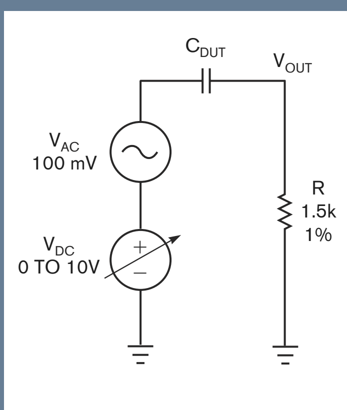


Figure A The model for the dc-test circuit consists of a variable dc-voltage source, an ac source of 100 mV rms, the capacitor under test, and a fixed resistor.

TABLE A
DEVICE-UNDER-TEST CAPACITANCE

DC-voltage applied (V)	−3-dB bandwidth (Hz)	C_{DUT} capacitance (μF)	Variance from 0V dc (%)
0	118.9	0.89	0
1	118.9	0.89	0
2	118.9	0.89	0
3	128.8	0.82	−7.7
4	138.7	0.76	−14.3
5	148.6	0.71	−20
6	158.5	0.67	−25
7	178.3	0.60	−33.3
8	188.2	0.56	−36.8
9	208	0.51	−42.8
10	237.8	0.45	−50

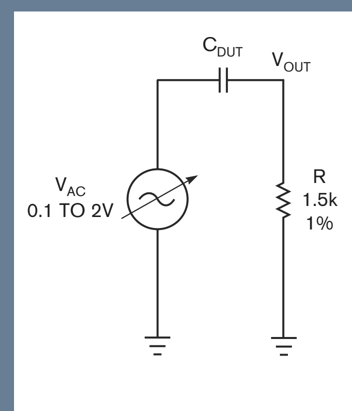


Figure C The model for the ac-test circuit is a simple series combination of a variable ac-voltage source, the capacitor under test, and a fixed resistor.

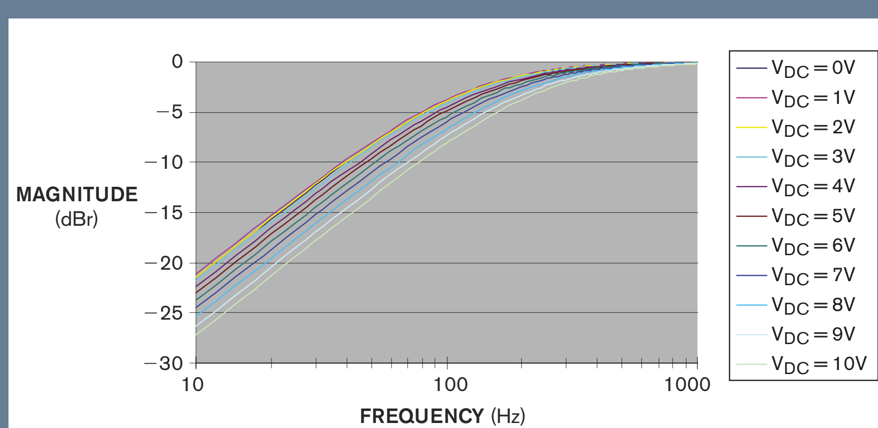
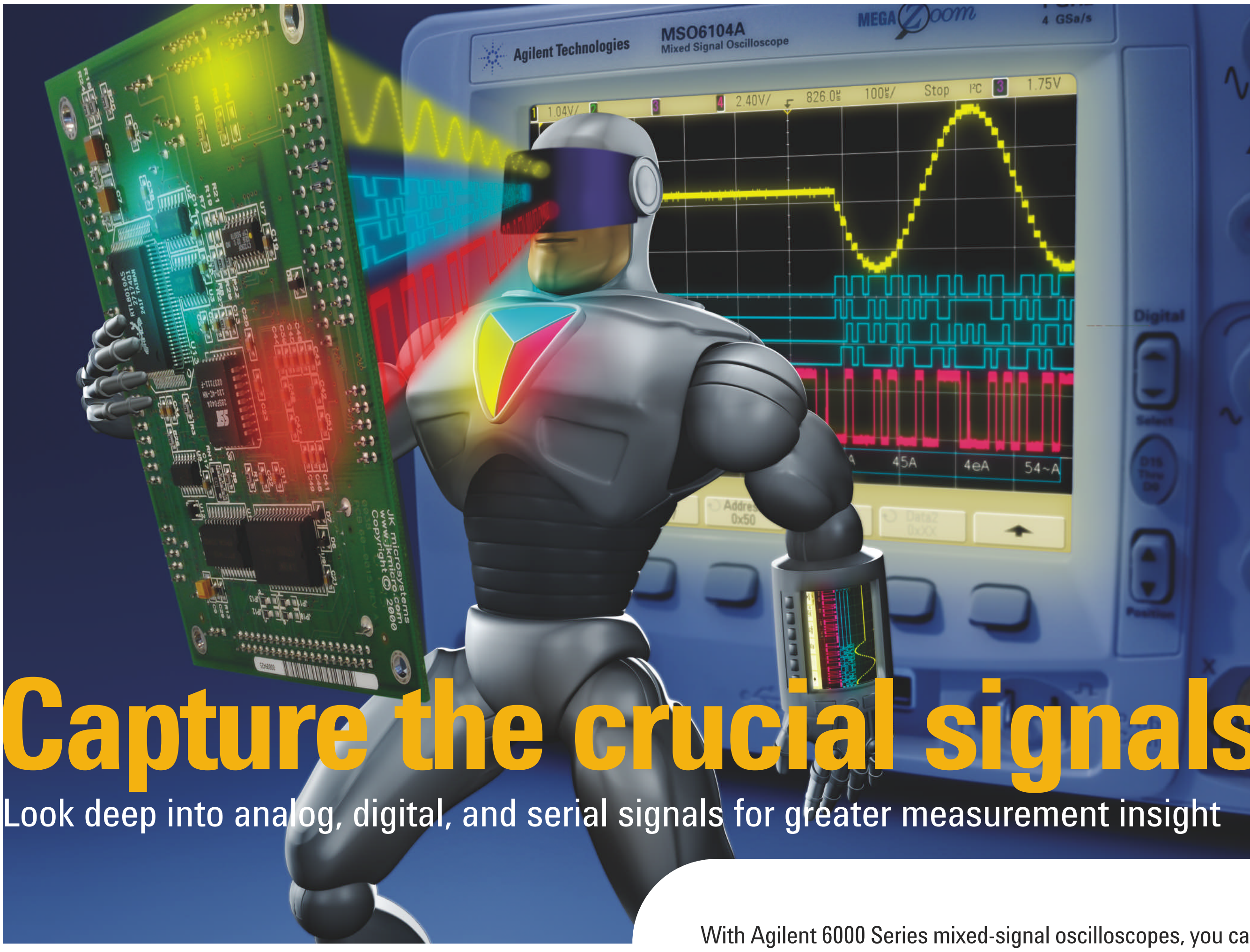


Figure B As you increase the bias voltage across the capacitor from 0 to 10V dc, the frequency response of the voltage across the resistor deteriorates—falling, at 100 Hz, from approximately 4 dB below its value at 1 kHz with zero bias to approximately 8 dB below with a 10V dc bias.



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dency of two capacitors with Y5V and X7R dielectrics, both with a 16V rating in a 0603 case. The dielectric material is now solely responsible for the difference in the voltage coefficient of capacitance. The X7R dielectric shows a 65 to 70% loss at the rated voltage. The Y5V dielectric exhibits a 70 to 80% loss over the rated-voltage range. **Figure 8** shows the variation in capacitance due to applied ac voltage for capacitors with Y5V and X7R dielectrics and a 16V voltage rating in an 0603 case.

Figures 7 and **8** illustrate an effect that translates into audio performance in **Figure 9**. You quantify the effect of applied voltage in terms of THD+N. A 1-μF, 0603-case ceramic capacitor with a 16V voltage rating is in series with a Maxim audio-amplifier input whose typical input impedance is 40 kΩ. C_{DUT} varies between an X7R dielectric and a Y5V dielectric as a THD+N Audio Precision sweep monitors the output distortion at frequencies of 20 Hz to 20 kHz. Notice the increased distortion at lower frequencies with the Y5V dielectric versus the X5R dielectric. The audio amplifier's decreasing loop gain limits the circuit distortion at frequencies greater than 1 kHz. Also notice that the THD+N in **Figure 9** begins to roll off above 6.3 kHz, because of the AES-17 (Audio Engineering Society) 20-kHz filtering at the analyzer's inputs. This measurement standard implements steep filtering above 20 kHz, attenuating any third-harmonic content above an input frequency of 6.33 kHz.

When considering capacitors for the audio-signal path, select capacitors with X7R dielectrics for better THD performance.

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Although X5R dielectrics outperform Y5V dielectrics, X7R dielectrics offer the best—that is, lowest—THD among Class 2 dielectrics.

The space, height, and cost restrictions typically associated with portable consumer electronics force the use of passive components with small footprints, low profiles, and low cost. When you use them for audio-signal coupling, some small-footprint, low-profile, low-cost passive components can limit low-frequency THD performance in audio circuits. However, doing so compromises audio sound quality and jeopardizes Vista compliance. Despite their slight footprint and price premium, large-footprint ceramic capacitors with high voltage ratings and X7R dielectrics are the best choice for all passive components in the signal path for a Vista-compliant audio design. EDN

REFERENCE

1 Microsoft, Windows Vista Logo Program Device Requirements, Version 3.0, www.microsoft.com/whdc/winlogo/hwrequirements.mspx#.

AUTHOR'S BIOGRAPHY

Kymberly Schmidt is a strategic applications engineer with Maxim Integrated Products, where she has worked for more than three years. She holds a bachelor's degree in electrical engineering from the University of California—Los Angeles and is responsible for audio-design support and for defining products that Maxim's multimedia-business unit will manufacture.

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BRIEF

Fully integrated TPS6300x buck-boost converter extends Li-ion battery life

By ***Bill Johns** • HPA Portable Power Applications*

Introduction

For portable power applications to take advantage of the small size and high energy density of modern battery technology, they must operate efficiently over the full battery-discharge voltage range. This presents a design challenge for Li-ion-powered systems requiring a 3.3-V bus. While standard buck converters excel at efficiently converting a 4.2- to 3.0-V Li-ion battery to lower output voltages such as 1.8 V, and standard boost converters efficiently convert an Li-ion battery to higher output voltages such as 5 V, neither provides an optimal solution for generating the ever-present 3.3-V bus. Topologies such as SEPIC and traditional buck-boost use the full battery capacity but suffer from drawbacks such as low efficiency, high cost, increased board area, and high part count. The TPS6300x, available in three configurations, can solve many of these problems. The TPS63000 has an adjustable output from 1.2 V to 5.5 V. The TPS63001 and TPS63002 outputs are fixed at 3.3 V and 5.0 V, respectively. All are available in the space-saving 10-pin QFN (DRC) package.

TPS63001

The Texas Instruments TPS63001 efficiently converts the Li-ion input to a 3.3-V bus with minimized part count, small board area, and reduced cost. It integrates both buck and boost functions into a single 3 x 3-mm QFN package, including switching FETs, compensation, and protection features. Only three external parts are required for operation: input and output capacitors and an inductor. The converter operates with a peak efficiency of 96% (see Figure 1). With a peak output current of 800 mA, it delivers enough current to power most portable loads. A wide input voltage range of 1.8 to 5.5 V allows operation with many popular power sources such as dual- and triple-cell alkaline and NiMH batteries as well as 3.3- and 5-V buses.

Figure 2 shows a typical 3.3-V supply that could be powered by a single Li-ion battery. A switching frequency of 1.5 MHz allows the use of a small 2.2-μH inductor and small 0603-sized ceramic input and output capacitors. High efficiency combined with a low external part count reduces the total solution size to only 6 x 6 mm (see Figure 3).

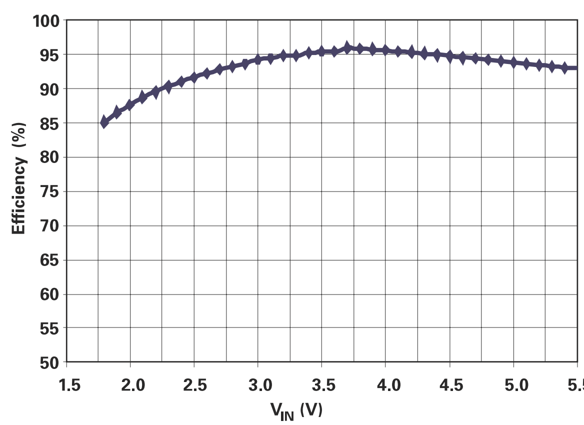

Figure 1. TPS63001 efficiency at 1.8- to 5.5-V with 320-mA load (V_{OUT} = 3.3 V)

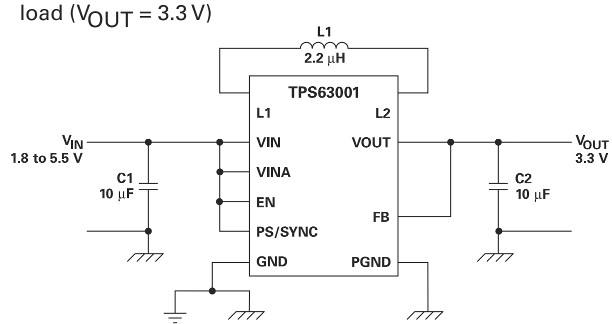

Figure 2. Typical application circuit

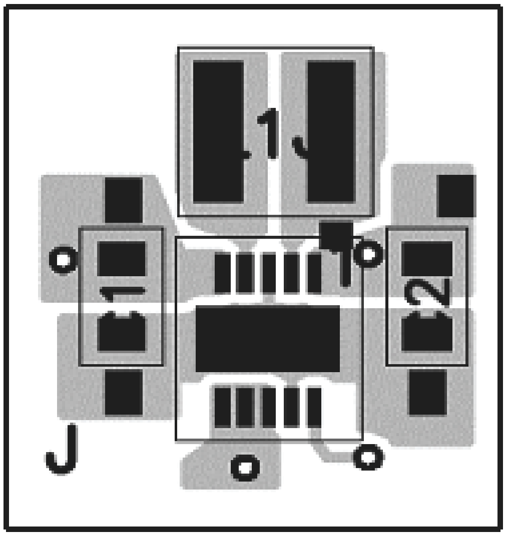

Figure 3. Typical layout in a 6 x 6-mm area

Advanced control topology maximizes efficiency

The TPS6300x is based on the standard H-bridge buck-boost power stage shown in Figure 4. It contains both buck and boost switching-FET configurations that are connected to a single inductor. Unlike a standard buck-boost mode that continuously switches all four FETs simultaneously, the TPS6300x uses a proprietary modulator design that switches only two FETs at a time. This control scheme significantly reduces unnecessary switching losses. The TPS6300x also reduces power loss by operating in the more efficient buck or boost mode rather than the traditional buck-boost mode.

As the Li-ion battery discharges down to and below 3.3 V, a buck-boost converter must transition from buck mode to boost mode. Many buck-boost control schemes exhibit efficiency drops, power-supply jitter, or unstable output voltage at this transition point. The TPS6300x transitions seamlessly between buck and boost modes on a pulse-by-pulse basis as necessary. This provides constant PWM switching over the buck and boost range with no overlap or dead time between the two modes.

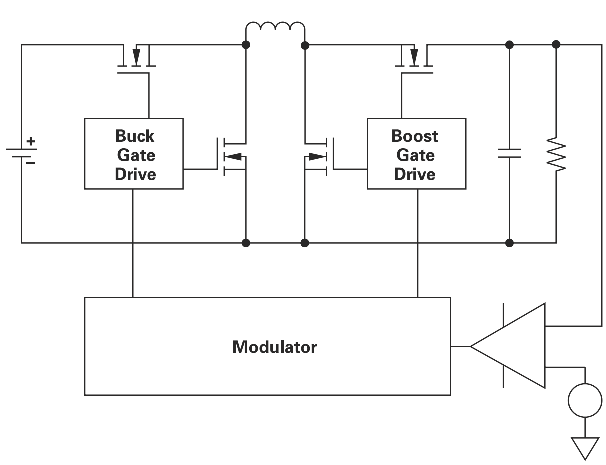

Figure 4. Block diagram of power section

Additional features

The TPS6300x contains additional integrated features that enhance its usability in portable applications that have, for example, an extremely low quiescent current (less than 50 μA), a user-selectable power-save (PS) mode that maintains efficiency at light loads, or external synchronization to help minimize system noise.

Average-current-mode control topology provides fast transient response and low output ripple in both buck and boost modes. Output regulation tolerance is ±1% over the input and load ranges. Internal compensation is optimized for an external inductor of 2.2 to 4.7 μH with an output capacitor between 10 and 22 μF.

Short-circuit protection provides a foldback current limit that reduces the output current limit from its maximum value of 1.7 A to 800 mA when the output voltage falls by 3%.

This reduces power dissipation on the device during an output overload condition. When the overload has cleared, normal operation resumes. One advantage of this approach is the ability to charge large-output capacitors such as super capacitors.

PS-mode features maintain very high efficiency, even at light loads below 300 mA. In the PS mode, switching occurs only long enough to raise the output voltage slightly above the output-voltage set point. Switching then stops until the output voltage falls below the set point again. This “on then off” switching provides excellent efficiency at light loads.

Other applications

The TPS6300x also operates in a current-regulation mode to drive a white-light-emitting diode (WLED). This is accomplished by replacing the output voltage divider network with a resistor in the return path of the WLED. Since the typical forward voltage drop of a WLED is 4.2 to 3.5 V, powering it from an Li-ion cell presents a problem to most power-supply topologies because the supply is required to both buck and boost its output voltage. The TPS6300x’s buck-boost functionality solves this problem and easily delivers 500 mA of current for a torch or flash application.

Conclusion

The TPS6300x is an ideal solution for converting an Li-ion battery to a 3.3-V bus. Its features such as high efficiency, small board area, low cost, and seamless transition from buck mode to boost mode make it an easy choice for the design engineer needing a high-performance design with quick turnaround.

References:

1. TPS61130 Synchronous SEPIC with Integrated LDO
2. TPS61060 Constant Current WLED Driver with Digital Dimming
3. TPS62110 High Vin Buck Converter


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How Matlab simplifies top-down design of closed-loop systems

A TOP-DOWN VIEW OF A CLOSED-LOOP SYSTEM'S CAPABILITIES AND PERFORMANCE LIMITATIONS SIMPLIFIES THE TASK OF SYSTEM DESIGN. READILY AVAILABLE SOFTWARE CAN HELP YOU TO OBTAIN THE NEEDED VIEW AND CONSTRUCT THE DETAILED MODELS THAT LEAD TO EFFICIENT DESIGNS.

Many applications in test and measurement take advantage of feedback to improve some aspect of performance. In simple power-sourcing instruments, for example, you can use the fact that, given the uncertain nature of the load, accurately measuring voltage is easier than forcing an accurately known voltage. As part of a feedback loop, a voltmeter can correct for IR drops and other errors to ensure that you apply to the load a voltage whose accuracy is as great as the meter's.

Feedback increases the dimensionality of the design problem, however. You must design not only for a particular function—dc gain in the case of the power source—to achieve the desired response, but also for the loop dynamics. Commonly, you control a feedback system's dynamics by controlling the location of its poles and zeros.

As an instructor of undergraduate control theory, I sometimes get calls from engineers in the field trying to figure out why their circuit isn't behaving as they would expect. The problems are usually evident in SPICE, but the symptoms don't always match well. Sometimes the SPICE frequency response looks OK, but the transient response isn't converging or is otherwise problematic. SPICE is a reasonable analysis tool to validate a design, but it is first important to verify that you design a system of dynamic elements according to plan—that is, that it is behaving in accordance with a top-down-design flow.

CONTROL THEORY

The primary task in feedback control is to design a controller, D, to manage a plant's dynamic behavior, G, despite uncertainty in the plant and the disturbance. (In control engineering, "plant" refers to a system that you are controlling.) Sensors, such as the voltmeter in the power-source example, monitor the plant's output. The difference between the desired and the measured outputs is the system error, E (**Figure 1**). You derive the basic equation of feedback control from an algebraic analysis of the **figure**.

$$Y = H_R \frac{DG}{1+DGH_Y} R + \frac{G}{1+DGH_Y} W. \qquad (1)$$

The bottom line is that feedback uses gain to reduce errors. A high gain in the controller creates a system whose output, Y, approaches the ratio of the forward and feedback transfer functions H_R/H_Y (outside and inside the loop, respectively), independent of parameter shifts within the plant, G, or of the disturbance, W.

But, as anyone who has experienced the squeal of a garage band's amplifier can attest, you need to be careful with gain and stability. Real circuits have poles and zeros that introduce delay and produce characteristic responses. The next thing on your to-do list should be to model the plant's dynamic behavior. You will work in the frequency domain, so you need a transfer function. The object of the modeling is to gain an understanding of the poles and zeros, or frequency response, of the plant that the sensor observes.

Finally, you design the controller as the last piece of the puzzle. The conflicting objectives are high gain for accuracy and low gain for stability. You resolve this conflict in the frequency domain, in which you can get high gain at low frequencies and you can roll off the gain at high frequencies before the phase shift approaches 180°.

The design of a feedback system in the frequency domain requires a close examination of the frequency response of the open-loop system. You can break the loop anywhere and insert a test signal. You use open-loop Bode magnitude and phase plots to determine closed-loop stability and bandwidth (**Figure 2**). The open-loop response, DGH_Y, appears in blue. From the **figure**, you deduce that the open-loop-gain magnitude

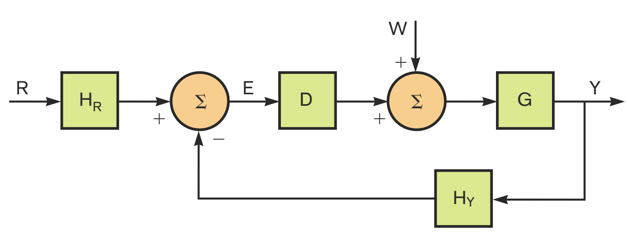

Figure 1 A feedback controller manages a plant's dynamic behavior to ensure stable operation and minimize the difference between the controlled system's desired and measured outputs.

passes through unity at about 12k radians/sec, which becomes the closed-loop bandwidth at the −3-dB point. At unity gain of 12k radians/sec, the open-loop phase is −101°. Thus, the closed-loop system's phase margin is 79°. The open-loop phase passes through −180° at 6.3k radians/sec. The gain at this frequency is −14.7 dB. Therefore, the system has 14.7 dB of gain margin.

Gain and phase margins measure the point of neutral stability—a condition just short of instability. A feedback-control system with open-loop gain of 1 and phase of −180° degrees oscillates when you close the loop around it. A gain stage in the controller allows you to move the open-loop magnitude curve up or down to appropriately adjust the gain and phase margins to avoid oscillation. The time-domain specifications and loop-gain drift requirements help you to decide how close to neutral stability to set the control gain.

To help ensure appropriate component selection, you can and should use SPICE analysis to determine the details of the system response in both the time and the frequency domains. Block-diagram analysis is part of a top-down-design method to ensure that your dynamic design—and not component-imposed limitations—establishes the system performance.

MATLAB

Deriving a transfer function for a first- or second-order system is fairly straightforward. Combining a system of dynamic transfer functions, such as you have in typical feedback-control applications, is a job for computer methods. Even if you find that you have a relatively high-order plant, you can generally break it into a series of first- and second-order elements. If you had determined that the plant's transfer function consisted of a dc gain of 0.85 and a second-order roll-off with a corner frequency of f_n=1 kHz with modest peaking, you would conclude that the Laplace transfer function was:

$$G(s)=\frac{0.85}{\left(\frac{s}{2\pi f_n}\right)^2+\frac{s}{2\pi f_n}+1}. \qquad (2)$$

You could create a Laplace transfer-function variable, G, in Matlab with the following syntax:

```
Gnum = [ 0.85 ];
Gden = [25.3e-9  159e-6   1];
G = tf(Gnum,Gden);
```

Matlab includes functions that accept transfer functions as input. The Controls toolbox contains functions to determine Bode plots and step response from the transfer function. For example, **Figure 3** shows the Bode and step-response plots from this plant.

Be careful with block-diagram algebra in Matlab. As you might expect, you can express the series connection of two transfer functions as the product of two transfer functions. However, you should use the feedback function to evaluate feedback that involves the division of transfer functions. Directly dividing transfer functions produces higher order results that look good in the time and frequency domains but can be difficult to evaluate as systems become more complex. For example, you can use the following statements to evaluate **Figure 1**'s input-output transfer function in the frequency domain:

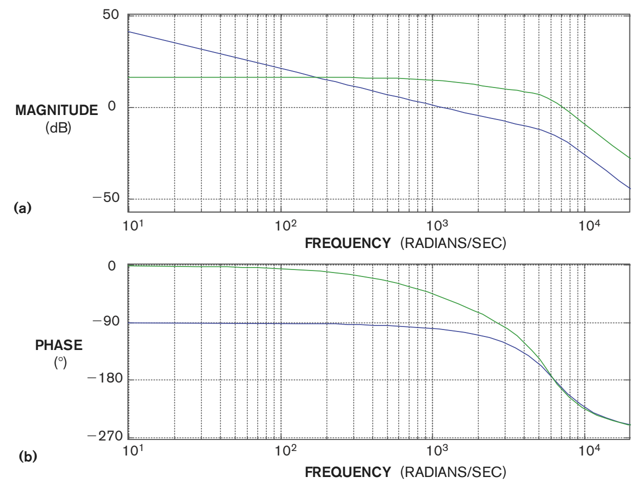

Figure 2 Bode plots show the magnitude (a) and phase (b) of system response as a function of frequency. The blue curves show the open-loop response of a typical system, and the green curves show the effect of feedback in the closed-loop response.

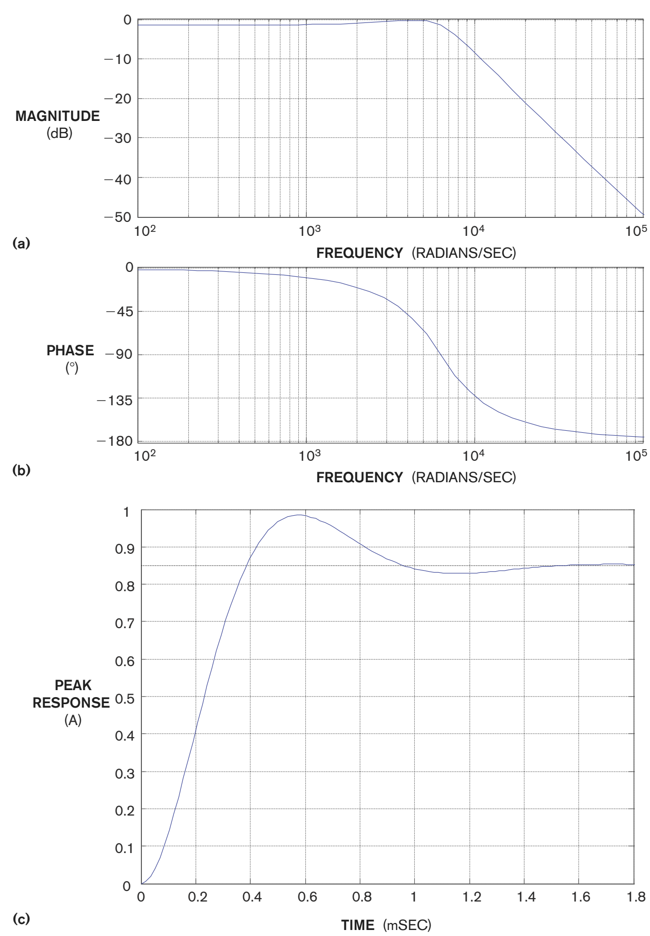

Figure 3 The Bode plots (a and b) and step response (c) of an example second-order plant exhibit some peaking in the frequency domain and overshoot in the time domain. The plant's dynamics influence your controller design.

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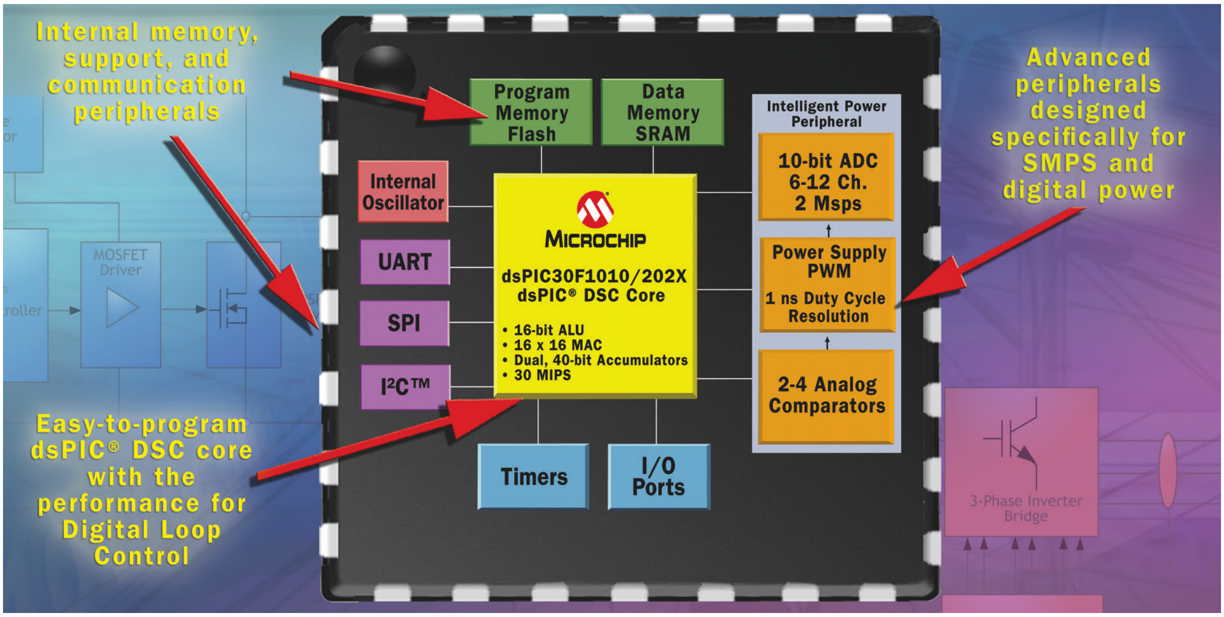

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```
bode(Hy*D*G);
% Open-loop frequency response
bode(Hr*feedback(D*G, Hy));
% Closed-loop frequency response
```

A time-domain analysis of the closed-loop-system step response is just as straightforward:

```
step(Hr*feedback(D*G, Hy));
```

You can use Matlab to capture the dynamic performance of each element of the control loop—using open-loop Bode plots as your guide—so that you achieve predictable and desirable closed-loop performance. You should limit manual analysis to low-order component modeling. With Matlab's transfer-function capabilities, you can combine the components into fairly complex systems.

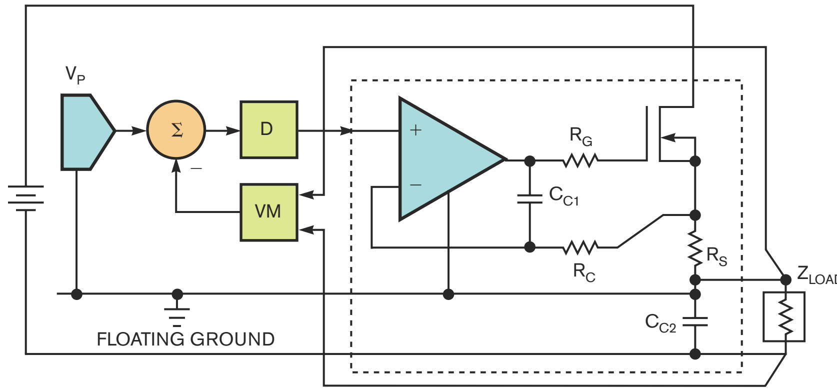

Figure 4 Among the key elements of this high-voltage power supply are the output amplifier, which the dotted line encloses, and the voltmeter, VM.

DESIGN EXAMPLE

Figure 4 shows a common high-voltage power-supply topology. This arrangement uses standard ±15V operational amplifiers to measure the output voltage and control the gate voltage of a high-voltage pass transistor. The topology requires some form of isolation, but the net result is that the control loop floats on the output level. Your job, with the help of Matlab, is the dynamic design of this system. Your customers will be thinking in terms of volts, amps, rise time, and overshoot. You need to convert the customer specifications into poles, zeros, and gain. But before you can apply the equations of control, you should break the circuit into more manageable blocks for analysis.

Start by developing a block diagram of the output amplifier, or plant. Modeling is a trade-off between detail and accuracy.

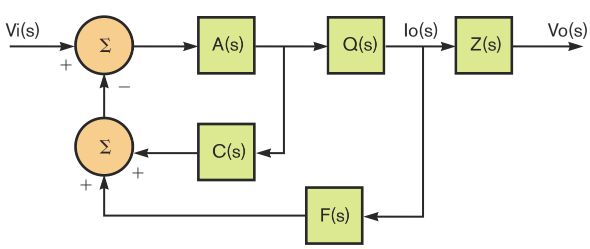

Figure 5 The plant's block diagram should include the operational amplifier, the output device, any necessary plant-compensation devices, and any significant parasitic elements.

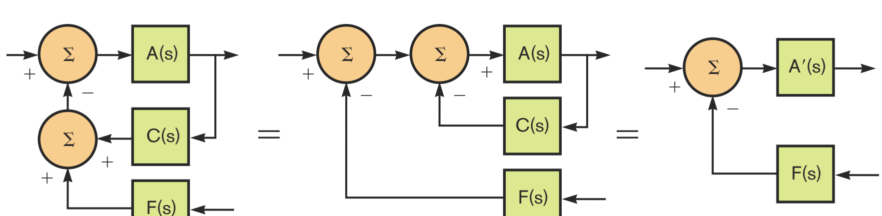

Figure 6 Using block-diagram algebra, you can simplify the component models that you use to represent the complete system.

A top-down approach starts at dc and includes dynamic detail out to and approximately 10 times beyond the frequency at which you close the loop at unity gain (the system's closed-loop bandwidth). By using SPICE to verify the design, you need to include only those elements that might affect the top-level design's phase and gain margins. Starting at dc, note that the floating amplifier is a voltage-controlled current source. Because you are interested in using this functional block as a voltage source, you need to include in your analysis the load impedance, which, though not a parameter that you typically can control, is one that you must include in the design analysis.

Besides the load, the plant's block diagram should include the operational amplifier, the output device, any necessary plant-compensation devices, and any significant parasitic elements (**Figure 5**). The initial analysis ignores MOS capacitance. You can add more detail once you have a functional model. As bad as it may look, the **figure** helps you to break the circuit into low-ordered components for modeling and analysis. The need for op-amp compensation and load compensation, C_{C1} and C_{C2}, becomes evident as you work through the power-supply dynamic analysis.

PLANT MODELING

The AD841 operational amplifier in this design has a typical open-loop dc gain of 45,000 and a typical gain-bandwidth product of 40 MHz. These values place the amplifier's low-frequency pole at roughly 900 Hz. The device-specification sheet also shows an open-loop Bode plot in which you can see additional poles at 100 MHz. The open-loop Bode plot shows more than 90° degrees of phase shift coming from the higher order dynamics, so you should assume the presence of at least a pair of complex-conjugate poles. Determining the damping factor is not critical for top-level dynamic design because you must avoid these poles' phase-shift contribution by closing the loop at a frequency significantly lower than that at which this contribution becomes significant.

You use component specifications

and circuit analysis to determine the transfer-function models of each of the plant's elements, as follows: For the op amp, Block A(s),

$$A(s)=\frac{A_0}{\left(\frac{s}{2\pi f_L}+1\right)\left(\left(\frac{s}{2\pi f_H}\right)^2+\frac{s}{2\pi f_H}+1\right)}. \quad (3)$$

For the output-transistor block, Q(s),

$$Q(s)=\frac{gfs}{1+gfs\times R_S}\Omega^{-1}. \quad (4)$$

The current-feedback block, F(s), is:

$$F(s)=R_S. \quad (5)$$

The load, Z(s) is:

$$Z(s)=R_L\left\|\frac{1}{sC_{C2}}\right.. \quad (6)$$

For the op-amp compensation network, C(s), the model is:

$$C(s)=\frac{s}{s+\frac{1}{R_C C_{C1}}}. \quad (7)$$

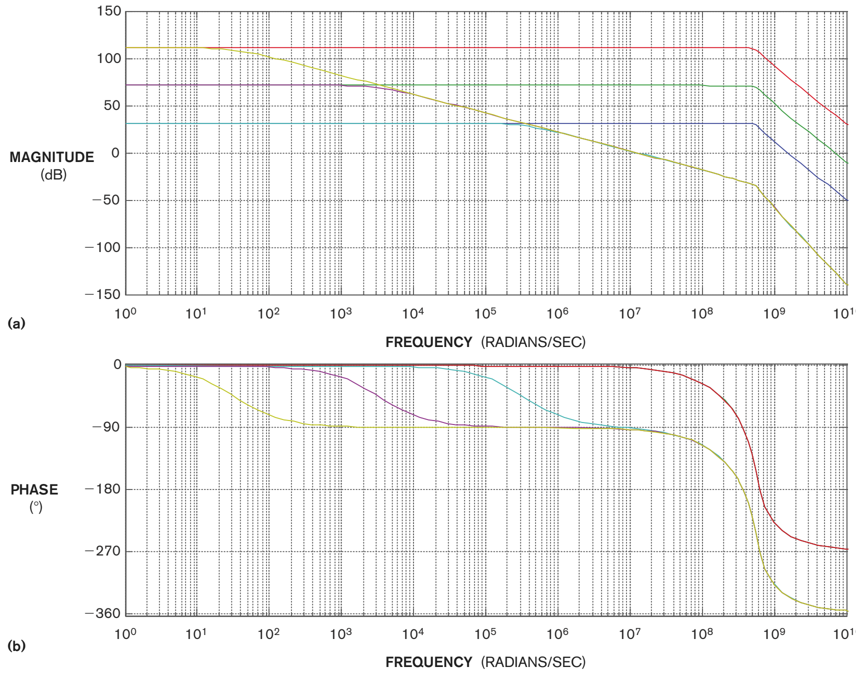

Figure 7 The output-amplifier closed-loop response depends on load resistance and whether you use load compensation. Compare the magnitude (a) and phase (b) response with load resistance of 100Ω (blue), 10 kΩ (green), and 1 MΩ (red) without C_{C2} with the yellow curve, which shows the response for all three values of load resistance with C_{C2} of 30 nF.

You might expect the unity-gain-stable AD841 to be fine in the follower configuration of this example. The only reason for including some amplifier compensation is dynamics—that is, phase shift—that the gate capacitance produces. You can capture the compensation within a modified amplifier model using some block-diagram algebra (**Figure 6** and **Equation 8**).

$$A'=\frac{A}{1+AC}. \quad (8)$$

Recall that Matlab provides a feedback function for evaluating transfer functions: Aprime=feedback(A,C). The source-degeneration resistor serves double duty by sensing the output current for the feedback loop, so the feedback is simply R_S, or 2.7Ω.

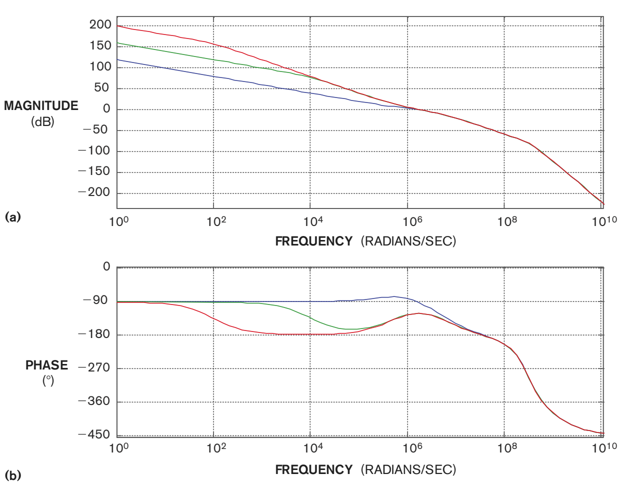

Figure 8 These magnitude- (a) and phase- (b) response curves depict the open-loop system response for the design example after appropriate controller design, with the same loading and color coding as those in Figure 7.

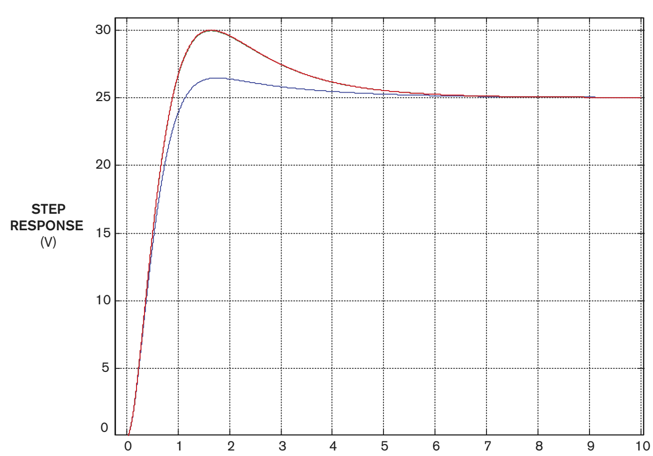

Figure 9 The closed-loop step response is identical for load resistance of 10 kΩ and 1 MΩ. With a load resistance of 100Ω, less overshoot exists because the open-loop gain is lower. (The color coding is the same as that in Figure 7.)

You can expect the MOSFET's dynamic characteristics to fall beyond the closed-loop bandwidth. You should, however, check that assumption with SPICE. As a start, model the MOSFET circuit simply as a fixed transconductance, linearized around its operating point. The model includes source degeneration of 2.7Ω and a nominal transistor transconductance of $2.5\Omega^{-1}$. Therefore, the output amplifier, the power-system plant, has a transfer function of

$$G(s)=\frac{V_O}{V_I}=\frac{A'QZ}{1+A'QF}. \quad (9)$$

DESIGNING THE CONTROL LOOP

The application of a current amplifier in a voltage-feedback control loop leads to loop gain that changes with load impedance, Z_L. As R_L increases, the closed-loop bandwidth increases, and the phase margin decreases until the point of oscillation. You need to add some capacitance, C_{C2}, in parallel with the output to force the amplifier bandwidth to decrease with predictable unity-gain crossover, independent of R_L. **Figure 7** shows the amplifier's Bode gain and phase response for three values of load resistor—100Ω, 10 kΩ, and 1 MΩ—with and without the compensation capacitor. Choose a 30-nF compensation capacitor to force a 2-MHz unity-gain crossing for the system's amplifier component.

Feedback (**Equation 1**) uses controller gain to drive the error signal toward zero. A typical controller uses an integrator because of its nearly infinite dc gain, which yields zero steady-state error. The problem with an integrating controller in this application is that it is adding another 90° of phase shift to a system already at 90° due to the plant's compensation. A reasonable step response requires at least 60° of phase margin, so you must incorporate a pole-zero pair to provide some phase lead near the system's open-loop unity-gain crossover.

$$D(s)=\frac{k}{s}\times\frac{s+z}{s+p}. \quad (10)$$

PARASITIC MODELING

Figure A presents a more complete block diagram, including poles from the gate resistor, B(s); MOSFET-input capacitance; and Miller feedback capacitance, M(s). For the gate-resistor model, B(s),

$$B(s)=\frac{1}{\frac{R_G C_{ISS}}{R_S g_{FS}+1}s+1}. \quad (A)$$

For the Miller capacitance, M(s),

$$M(s)=\frac{s}{s+\frac{1}{R_G C_{RSS}}}. \quad (B)$$

The project's selected MOSFET, an International Rectifier IRF830, has a gate capacitance of 600 pF. A 47Ω resistor isolates the op amp from this capacitance during transition periods. This source degeneration reduces the gate resistor's impact. The IRF830 specification suggests approximately 10 pF of drain-to-gate capacitance. Whether the model needs to include this capacitance in modeling against a 47Ω gate resistor at a planned voltage gain of 25 is questionable, but this discussion includes Miller capacitance for completeness.

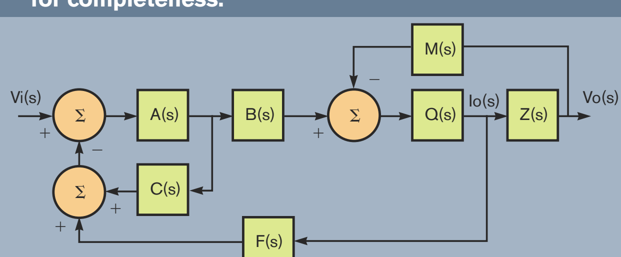

Figure A A more complete model of the output amplifier includes poles from the gate resistor, B(s); MOSFET-input capacitance; and Miller feedback capacitance, M(s).

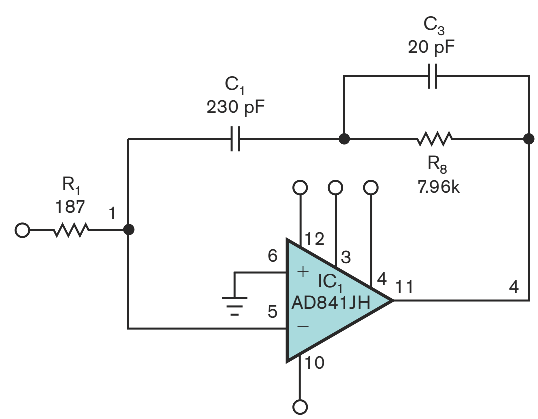

Figure 10 More detailed modeling reveals more overshoot and ringing.

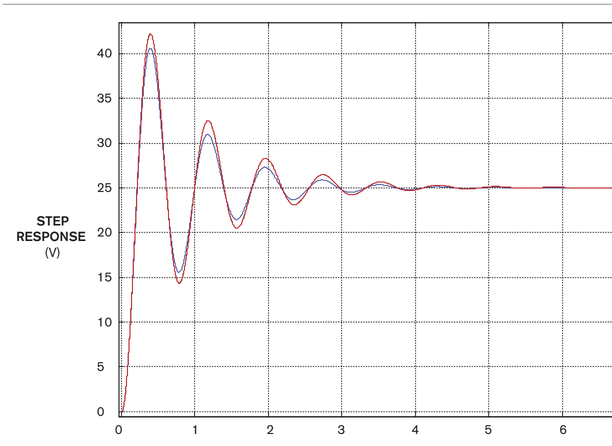

Figure 11 The closed-loop-system step response shows more ringing when the controller design includes a real op-amp model.

You are designing for a closed-loop gain of 25. Therefore, the voltmeter, H_Y, produces a nominal gain of 1/25, or 0.04. Bandwidth adds value in instrumentation, but you must be careful with the plant's rapid phase shift starting at approximately 3 MHz. So, target a closed-loop bandwidth of 300 kHz. Place the phase-lead zero at 80 kHz and the pole at 1 MHz. Matlab determines a controller gain of 23.3M, placing the unity-gain crossover at 300 kHz. **Figure 8** shows the open-loop Bode plots, and **Figure 9** shows the closed-loop step response expected from the power-supply system under the three load-resistance values evaluated throughout the design. The important feature is the consistency of unity-gain crossover versus load resistance. The compensation scheme holds closed-loop dynamics constant from a load resistance of 400Ω to infinity. Lower load resistance starts to reduce loop gain but, by so doing, improves system stability.

The top-down design of a power-supply control system is now complete. You should not be surprised to find, however, that a prototype or a SPICE analysis of the resulting circuit exhibits less phase margin, more ringing, and more overshoot than you predicted. This behavior occurs because the analysis pushed the bandwidth into unmodeled territory. You could have included the dynamics of the gate resistance and capacitance and the Miller capacitance (see **sidebar** "Parasitic modeling"), but the topology and voltage-feedback- compensation capacitor, C_{C2}, reduces loop sensitivity to these high-order dynamics. The key to closing this design is to realize that the controller, D, is implemented in an op-amp circuit (**Figure 10**). Additional phase shift from the op amp's poles reduces the overall phase margin. The full system step response in **Figure 11** compares reasonably with SPICE analysis once the controller model includes the dynamics from its op amp. You can download Matlab code for this example from www.merrimack.edu/generator.php?id=2495. **EDN**

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AUTHOR'S BIOGRAPHY

William Bowhers received a master's degree in electrical engineering from Boston University and a bachelor's degree in electrical engineering from Villanova University (Villanova, PA). He is an assistant professor of electrical engineering at Merrimack College (North Andover, MA), teaching signals and systems, probability, and control theory. His research projects support a general interest in measurement technology, acquired through 25 years of instrumentation development at Teradyne Inc (North Reading, MA). Current projects include low-noise power conversion and field-programmable CMOS analog circuits. He is a member of the IEEE and ASEE (American Society for Engineering Education).

LINEAR TECHNOLOGY

DESIGN NOTES

Wide Input Voltage Range Buck-Boost Converter Simplifies Design of Variable Input Supplies – Design Note DN413

John Canfield

Introduction

Many of today's portable electronic devices require the ability to operate from a variety of power sources including USB, wall adapters, and alkaline and lithium batteries. Designing a power conversion solution that is compatible with this wide array of power sources can be daunting. The LTC®3530 monolithic synchronous converter simplifies the task by operating in both buck and boost modes over an extended input voltage range of 1.8V to 5.5V. No complicated topology is required to account for varying inputs that can be above, below or equal to the output.

The LTC3530 utilizes a proprietary switching algorithm that provides seamless transitions between buck and boost modes while simultaneously optimizing efficiency over all operating conditions. Using this advanced control algorithm, the LTC3530 is capable of high efficiency, fixed frequency operation with input voltages that are above, below, or equal to the output voltage, while requiring only a single inductor. This capability makes the LTC3530 well suited for lithium-ion/polymer and 2-cell alkaline or NiMH applications which require a supply voltage that is within the battery voltage range. In such cases, the high efficiency and extended input operating range of the LTC3530 offer greatly improved battery run-time, as much as 25% in some cases, over alternative solutions.

At 3.3V output, a load current of up to 600mA can be supported over the entire lithium-ion input voltage range; 250mA of load current is supported when the input is 1.8V. The output voltage is user-programmable from 1.8V to 5.25V via an external resistor divider. The LTC3530 includes a soft-start circuit to minimize the inrush current transient during power-up. The duration of the soft-start period can be programmed via the time constant of an external resistor and capacitor.

The switching frequency of the LTC3530 is user programmable via a single external resistor, allowing the converter to be optimized to meet the space and efficiency requirements of each particular application. An external resistor and capacitor provide compensation of the feedback loop, enabling the frequency response to be adjusted to suit a wide array of external components. This flexibility allows for rapid output voltage transient response regardless of inductor value and output capacitor size.

The LTC3530 features an automatic transition to Burst Mode® operation at a user programmable current level to improve light load efficiency. For noise sensitive applications, the LTC3530 can be forced into fixed frequency operation at all load currents by connecting the BURST pin to V_{IN}. The LTC3530 also features short-circuit protection and overtemperature shutdown. Internal reverse current limiting circuitry prevents damage to the part should

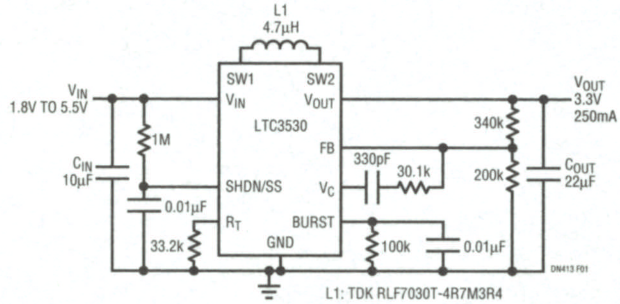

Figure 1. 3.3V at 250mA from a 1.8V to 5.5V Input

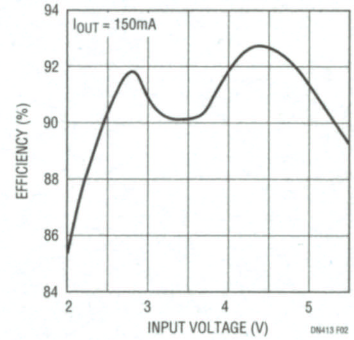

Figure 2. Efficiency vs Input Voltage of the Circuit in Figure 1

the output voltage be pulled above regulation through an external path.

Efficiency

Figure 1 illustrates a typical LTC3530 application circuit configured with a 1MHz switching frequency, which represents a good compromise between the PCB area and efficiency for most applications. The efficiency curve versus input voltage for this application circuit is shown in Figure 2. The LTC3530 achieves greater then 85% efficiency with an input voltage greater than or equal to 2V. These high levels of efficiency in combination with its wide input voltage range make the LTC3530 an attractive solution for battery-operated products and other efficiency-sensitive applications.

Programmable Burst Mode Operation

The LTC3530 provides automatic Burst Mode operation, which greatly improves efficiency at light load currents. Burst Mode operation reduces the operating current of the LTC3530 to only 40µA in order to improve light load efficiency and extend battery runtime. The LTC3530 automatically transitions to Burst Mode operation when the average output current falls below a user programmable level set via an external resistor. When the load current rises above the Burst Mode threshold, the part automatically returns to fixed frequency PWM operation.

The precise control circuitry of the LTC3530 allows the Burst Mode threshold to be set at load currents as low as 20mA. In addition, the LTC3530 directly monitors the average load current thereby providing a Burst Mode transition threshold that is independent of input voltage, output voltage, and inductor value, unlike other devices that rely on the level of peak inductor current.

In noise sensitive applications, the LTC3530 can be forced into fixed frequency PWM operation at all load currents by simply connecting the BURST pin to V_{IN}. In addition, the BURST pin can be driven dynamically in the application to provide low noise performance during critical phases of operation, or to reduce voltage transients during periods of expected large load transitions.

1.27mm Profile Li-Ion to 3.3V Regulator

The high switching frequency and advanced buck-boost switching algorithm of the LTC3530 allow the use of small external components. Figure 3 shows a circuit that is optimized to reduce the total application size. The entire converter has a maximum height of 1.27mm and occupies a PCB area of only 0.135 square inches making it ideal for height constrained applications such as PC cards. Figure 4 shows the efficiency versus input voltage for this area-optimized application circuit. This converter is able to support a 600mA load for output voltages above 2.4V and obtains greater than 86% efficiency over the entire Li-Ion input voltage range.

Conclusion

The LTC3530 with its high efficiency, wide input voltage range, and tiny circuit size is well suited to a variety of battery operated products and other efficiency-sensitive applications. With the IC's array of programmable features, the circuit can be customized to meet the needs of any application, while still maintaining a compact total solution footprint.

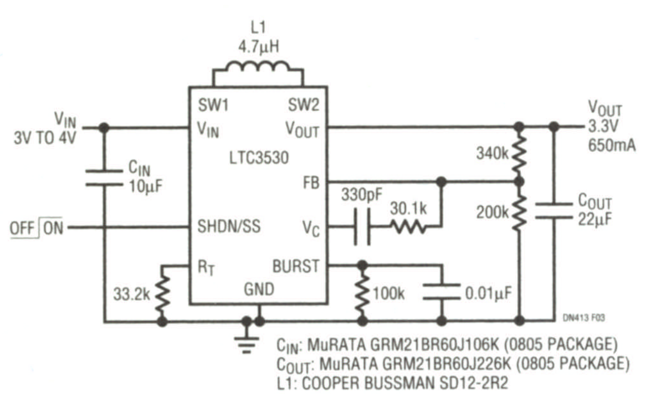

Figure 3. 1.27mm Profile and Area Optimized Application Circuit

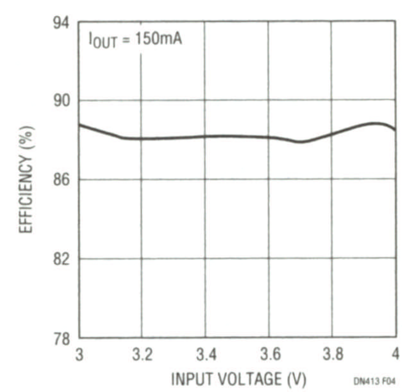

Figure 4. Efficiency vs Input Voltage of Figure 3 Circuit

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Real-world power tests model FPGA's thermal characteristics

Jeremy Willden, Ad Hoc Electronics, Pleasant Grove, UT

Given ever-increasing clock frequencies and higher gate counts, many systems that include high-performance FPGAs (field-programmable gate arrays) routinely require a thoroughly analyzed thermal model. While working on a project that contained an FPGA, I realized that I had insufficient data to determine the FPGA's exact power dissipation, which my mechanical-engineering colleague required to construct a system model for thermal analysis using Flomerics' (www.flomerics.com) Flotherm software.

Although we had created fully functional hardware, we hadn't included a method of measuring the FPGA's exact power consumption, a problem further complicated by the presence of multiple power-supply voltages that fed additional circuits on the board. Although the manufacturer's FPGA-power-calculation spreadsheet allowed us to approximate the circuit's total wattage, the calculated values related only to its internal power consumption and didn't account for power not dissipated in the chip—that is, power delivered to I/O lines that drive other devices. To further confuse the issue, we lacked information about the FPGA package's thermal properties.

My mechanical-engineering colleague and I decided to create a controlled experiment by placing a functioning PCB (printed-circuit board) inside an improvised temperature chamber—a cardboard box. We would apply a precise amount of power only to the FPGA, measure its package's external temperature, and measure its internal die temperature using the FPGA's on-chip temperature-sensing diode. We would then model the experiment in Flotherm and adjust the package's thermal properties until the simulation's results matched the measurements.

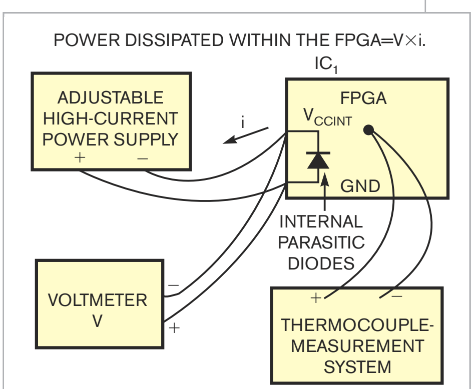

Figure 1 To measure an FPGA's thermal parameters, apply controlled forward bias to its internal parasitic diodes, thereby dissipating a known amount of power within its die.

Next, we would measure the FPGA's temperature while it executed an actual VHDL application within the temperature-controlled environment and work backward to determine the true power dissipation. Finally, we would create an accurate Flotherm model that would allow completion of a properly rated heat-sink design for the FPGA.

The only nonobvious part of this process involved how to dissipate a controlled amount of power within the FPGA. Acting on a flash of inspiration, I connected a nonfunctional PCB to a power supply and reversed the polarity of the FPGA's core voltage. By doing so, I applied forward bias to the FPGA's internal parasitic diodes that connect between power and ground and the device's I/O-voltage rails and protection diodes (**Figure 1**). Under normal circumstances, these diodes remain reverse-biased and dissipate no power. Reversing the power-supply polarity forward-biased the diodes, dissipating power and heating the FPGA's die.

To obtain an exact voltage measurement, I added Kelvin-connected sense leads to the FPGA's power pins. I configured the power supply to operate in constant-current mode and adjusted its output to deliver exactly 2W of power as determined by multiplying the supply current and the voltage at the FPGA's power pins. My colleague configured the test probes' placement and performed the temperature measurements. Upon completion of our experiments, the temperatures that the Flotherm model predicted agreed with those we measured in our system's final configuration, including its heat sink, within a margin of 3 to 4°C. EDN

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CPLD autonomously powers battery-powered system

Rafael Camarota, Altera Corp, San Jose, CA

A common industrial and consumer application is a system that samples an environmental condition, such as GPS (global-positioning-system) location, voltage, temperature, or light, at a wide interval, such as once every minute. This type of system is becoming increasingly wireless and battery-powered; it wakes up every minute, takes a sample, transmits data to a central data-collection terminal, and then goes back to sleep. This Design Idea uses a small portion of an Altera (www.altera.com) EPM240-T100 CPLD (complex programmable-logic device) with a few discrete capacitors, resistors, diodes, and MOSFETs to autonomously wake a CPLD-based system from a full power-down state to an on state using an RC-timer circuit. This approach results in minimal

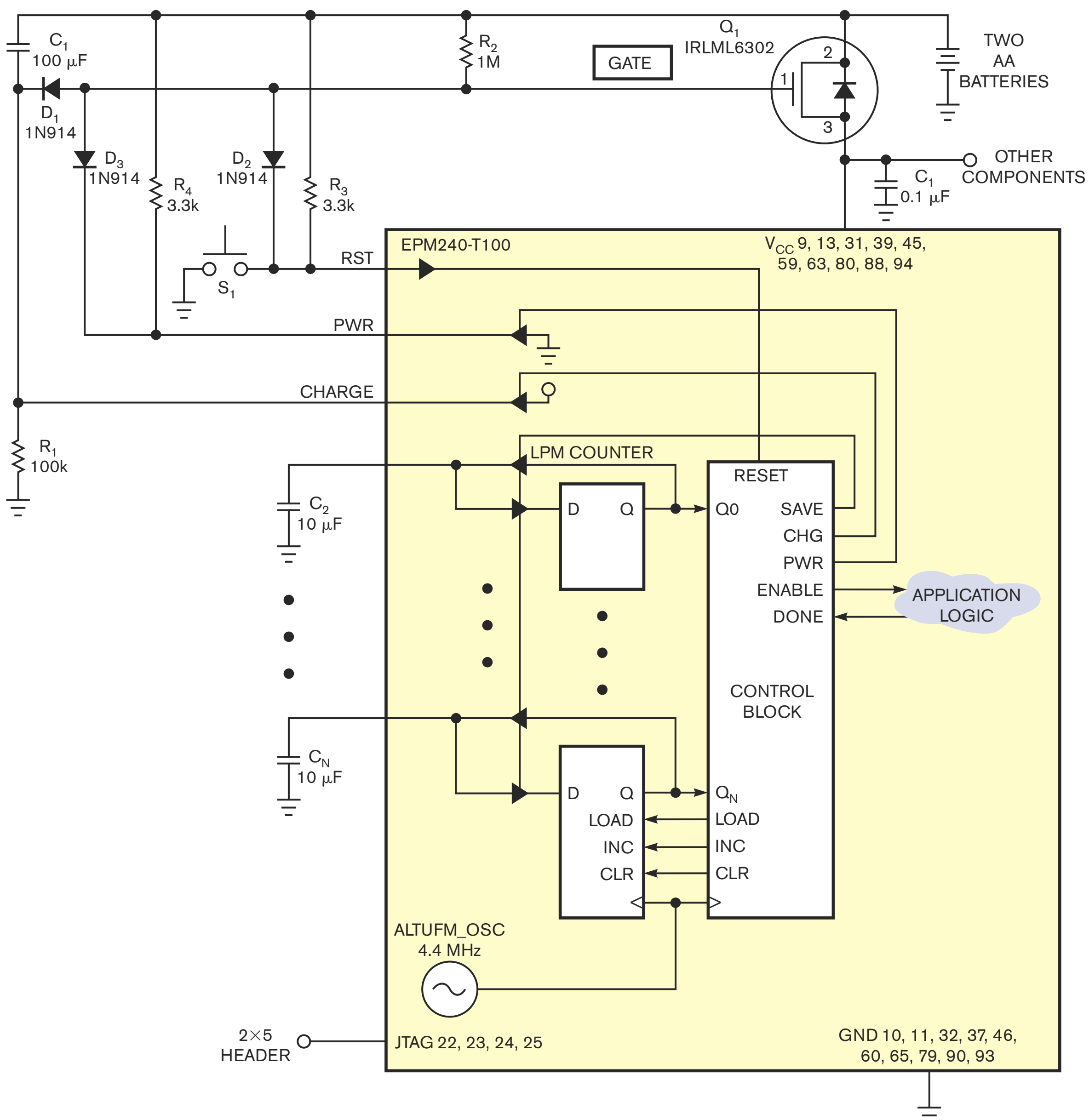

Figure 1 The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

power consumption during samples when the power is on and between samples when the system, except for the RC circuit, is effectively off.

Figure 1 shows the basic CPLD on/off timer. Q_1, an IRLML6302 P-channel MOSFET, is the power-control switch for the system. When the gate node is at V_{CC}, which R_2 pulls up, the power to the CPLD and the entire system is off, leaving only the RC circuit to use a minute amount of power. The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

Figure 2 shows the state machine of the control block. The outputs in the state box are high, and all others are low. The dashed line from power-down to power-up represents the time delay, which the RC circuit comprising R_1 and C_1 measures when the system is off. Switch S_1 turns on and initializes the circuit. When S_1 closes, D_2 drives the gate node low, consequently turning on Q_1 when the gate voltage is 0.7V below V_{CC}. The EPM240-T100 is then operating in the power-up state less than 200 μsec after Q_1 applies power. The power-up state drives the power node low, which holds the gate voltage at 0.7V, keeping Q_1 on after the switch is open. The power-up state also drives the charge node to V_{CC}. This action charges the negative terminal of C_1 to V_{CC}. Because reset=0, the control block goes to the reset state and Register 1 gets reset. Once S_1 opens, the control block goes to the enable state and drives the enable signal to one.

The sample-and-transmit circuit then begins operation and drives the done signal to zero. Once the sample and transmit are complete, the done signal becomes one, and the control block goes to the save state. The save state charges capacitors C_2 to C_N based on the value in Register 1. The

CAPACITORS C_2, C_3, AND C_4 ACT AS NONVOLATILE MEMORY, STORING THE COUNT OF PREVIOUS POWER CYCLES.

save state is active for 100 μsec, allowing the outputs to fully charge the 10-μF capacitors. After 100 μsec, the control block goes to the power-down state, which stops driving the charge and power nodes. R_4 pulls the power node high, leaving R_2 to pull up the gate node.

Once the gate node reaches $V_{CC}-V_{TQ1}$ at about 2.3V, Q_1 shuts off power to the system. All EPM240-T100 I/O is in a high-impedance state and does not affect the gate or charge nodes. The charge node starts at V_{CC} and begins to discharge through R_1 once power is off. Once the charge node drops to 2.3V, D_1 pulls down the gate node. Once the charge node reaches 1.6V, the gate node reaches 2.3V, and Q_1 turns on. The time for Q_1 to turn on is slightly less than the τ of R_1 and C_1. Off time equals $R_1 \times C_1 = 100{,}000 \times 0.0001 = 10$ sec.

The device powers up in the power-up state but moves quickly to the sample state. The sample state reads the value on capacitors C_2, C_3, and C_4. These capacitors act as nonvolatile memory, storing the count of previous power cycles. If the Register 1 value sampled on C_2 through C_4 is less than 7, then the control block goes to increment, and the Register 1 value increments by one. Then, the control block again goes to the save state to charge C_2 through C_4 to a new binary value, 001. The device powers down again. On the eighth power cycle, or about 80 seconds after power-up, the control block moves to the enable state, thus enabling a new sample-and-transmit sequence. This process repeats every 80 seconds. You can change the period by adjusting C_1 and R_1 and by changing the Register 1 size and count between enable cycles. Based on an 80-second period comprising eight smaller power-up samples, test, and power-down cycles, the duty cycle for power is less than 3%; therefore, this approach increases battery life by as much as 33 times. **EDN**

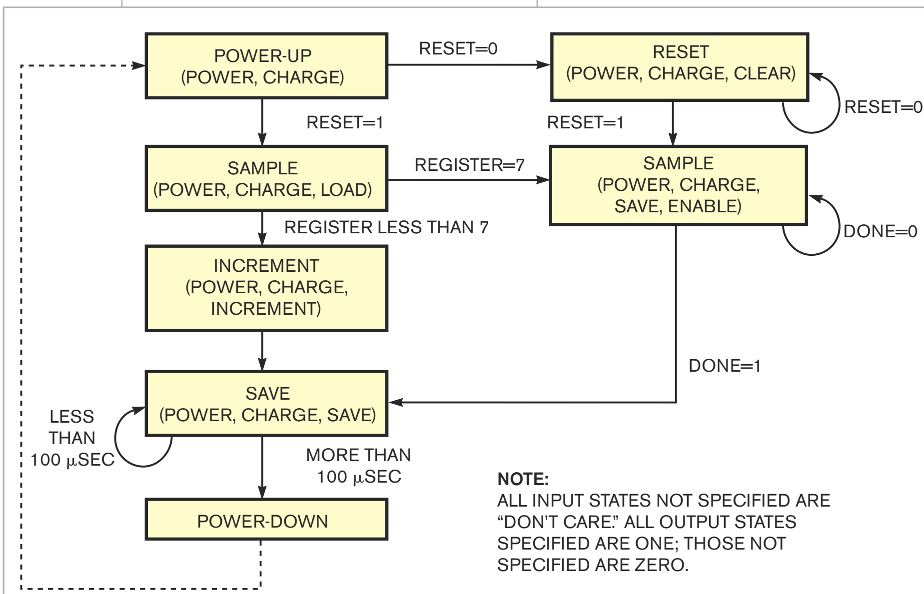

Figure 2 In the state machine of the control block, the outputs in the state box are high, and all others are low.

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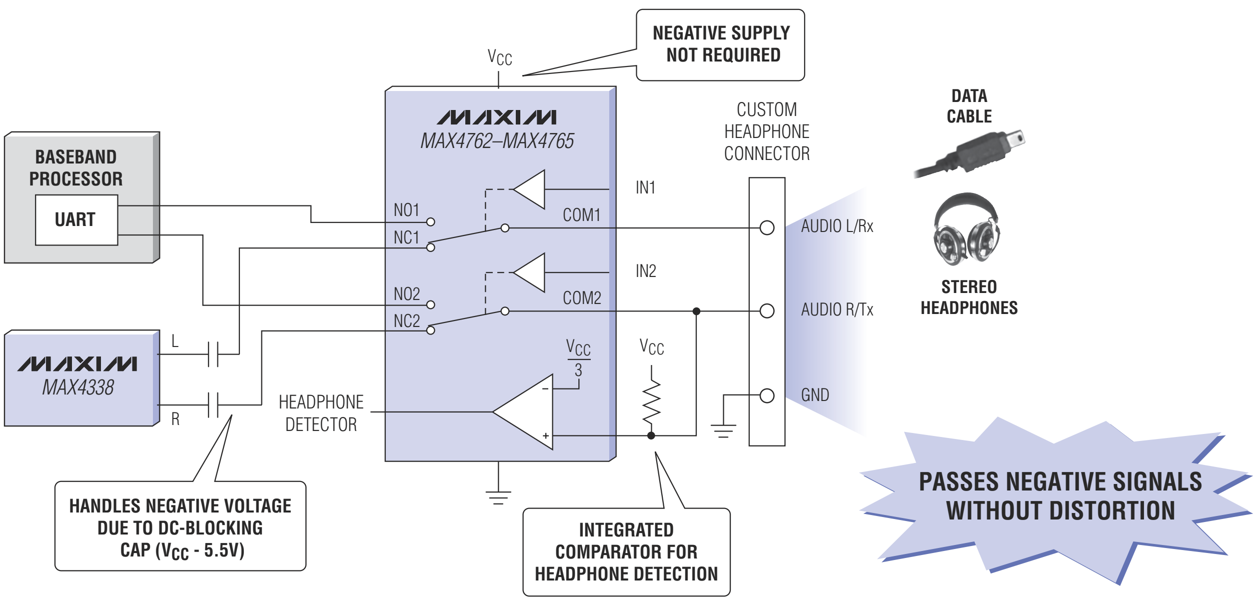

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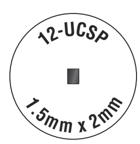

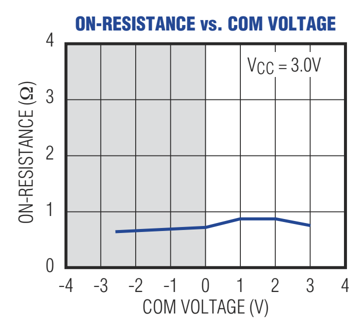

Part	Function	R_{ON} (Ω)	R_{ON} Flatness (Ω, max)	Comparator	Shunt Switch	Supply Voltage (V)	Package
MAX4762	Dual SPDT	0.4	0.3	No	No	+1.8 to +5.5	10-µMAX®/TDFN/12-UCSP™
MAX4763	Dual SPDT	0.4	0.3	Yes	No	+1.8 to +5.5	12-UCSP/QFN
MAX4764	Dual SPDT	0.4	0.3	No	Yes	+1.8 to +5.5	10-µMAX/TDFN/12-UCSP
MAX4765	Dual SPDT	0.4	0.3	Yes	Yes	+1.8 to +5.5	12-UCSP/QFN

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Find hex-code values for microcontroller's ADC voltages

Harry Gibbens Jr, Deafworks, Provo, UT

This Design Idea is for low-end, eight-pin, flash-memory, 8-bit microcontrollers, such as the MC68HC908QT4A from Freescale (www.freescale.com), but it would apply to any 8-bit microcontrollers that use the ADC feature. In a nutshell, the ADC converts an input-analog-voltage level to a digital-signal format. The digital-signal format has an 8-bit hex-code value, such as $00. The microcontroller "sees" the input-analog-voltage level from its ADC ports ranging from $00 at V_{SS} to $FF at V_{DD}. Based on those hex-code values, there are a total of 256 ticks. The input voltages between V_{SS} and V_{DD} represent a straight-line linear conversion. In other words, the higher the input voltage, the higher the hex-code value.

The difficulty is that a programmer who needs to write assembly code for a programming algorithm must know what the hex-code value is for a different input-analog-voltage level—1.6V, for example. Referring to the microcontroller's specs and even contacting its manufacturers do not yield satisfactory answers.

However, this Design Idea presents a solution to the problem. Given the microcontroller's power operating-voltage source, V_{DD}, use the following simple formula to obtain the hex-code value corresponding to an identified input-analog-voltage level: $V_{IN} \times V_{IN}/(V_{DD}/255)$=result value=hex code. Note that you must round off the result value to a whole number before converting to a hex-code value for better accuracy. The following sample calculation finds the hex-code value for a measured input-analog-voltage level of 1.6V when using a known microcontroller's V_{DD} of 5V: 1.6V/(5V/255)=81.6=82, or $52. **EDN**

Cheap and easy inductance tester uses few components

Al Dutcher, Consulting Engineer, Paulsboro, NJ

In the absence of expensive test equipment, the circuit in **Figure 1** offers a simple and rapid alternative method of measuring inductance. Its applications include verifying that an inductor's value falls close to its design parameters and characterizing magnetic cores of unknown parameters that accumulate in the "junk box." As designed, the circuit tests most inductors for use in power supplies and many inductors for RF circuits.

The circuit comprises two cascaded common-emitter-amplifier stages that form a nonsaturating, cross-coupled flip-flop. A common-emitter stage performs a phase inversion, and two cascaded stages form a noninverting feedback amplifier with gain that produces regeneration. Without the presence of the inductor that is undergoing test, L, regeneration occurs at dc, and the circuit behaves as a bistable flip-flop that assumes either of two stable states. Connecting the inductor reduces the dc positive feedback to below the regeneration level. Thus, regeneration can occur only at ac, and the circuit becomes an astable oscillator.

Keeping the transistors out of saturation speeds the circuit's operation by minimizing the transistors' storage time. Although virtually any type of high-speed, small-signal RF transistor provides adequate switching speed, lower frequency devices also work but decrease the low-inductance-measurement range. The circuit's frequency of oscillation is inversely proportional to the inductance that is undergoing test, and you can use either a frequency counter or an oscilloscope to measure the frequency of oscillation.

Figure 2 shows the waveform produced by an inductor with a value of approximately 100 μH. The frequency of oscillation depends on the L/R time

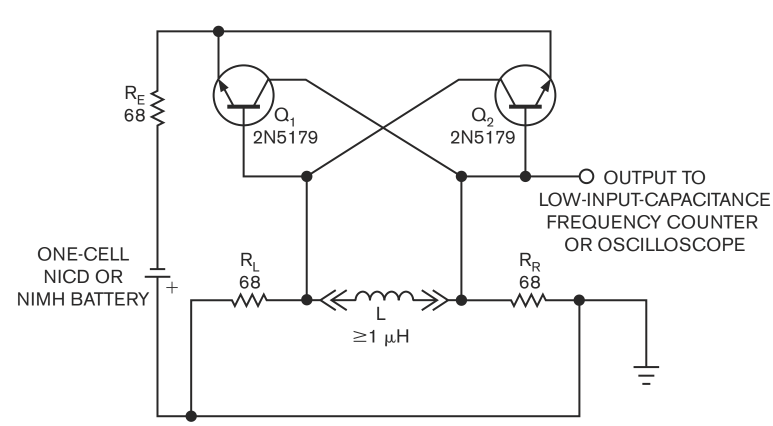

Figure 1 An inductance-test oscillator comprises two transistors and a few passive components. (Editor's note: For best results, minimize the lengths of all components' leads.)

constant comprising the inductance under test and resistors R_L and R_R. The time the waveform takes to change its state is directly proportional to the inductance, and, for one-half cycle, it approaches T_{HALF}=L/100. The period of a full oscillation cycle is twice that amount, or T_{FULL}=L/50. Solving for the inductance yields L=50×T_{FULL}. As an alternative, the frequency is inversely proportional to the inductance, or f_{OSC}=50/L. Using a frequency counter allows measurement of inductance as L=50/f_{OSC}.

The circuit's finite switching speed of approximately 10 nsec imposes a lower floor of 1 μH on its measurement range. You can measure a small inductance by connecting it in series with a larger inductance, noting the reading, measuring the larger inductance alone, and subtracting the two measurements.

Although the circuit imposes no upper limit on inductance values, when the inductor's ESR (equivalent-series resistance) exceeds approximately 70Ω, the circuit stops oscillating and reverts to bistable operation. The circuit measures values of all inductors and transformer windings except for small, low-frequency iron-core devices that present a high ESR. For greatest accuracy, use a low-input-capacitance instrument to measure the frequency of oscillation.

A single NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) rechargeable cell provides power for the circuit. These cells present a relatively flat voltage-versus-time discharge characteristic that enhances the circuit's measurement accuracy. The circuit consumes approximately 6 mA during operation.EDN

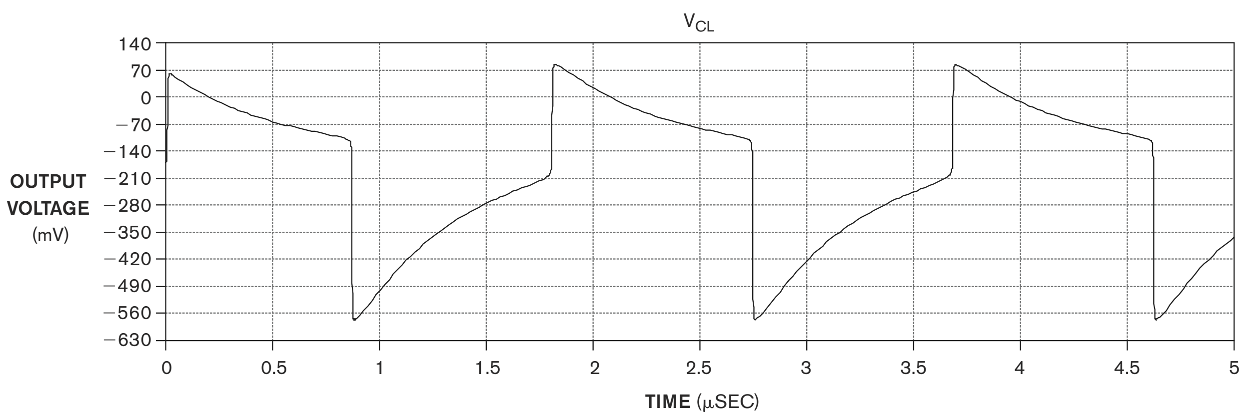

Figure 2 Testing an inductor with a value of approximately 100 μH produces this output waveform.

Add a manual reset to a standard three-pin-reset supervisor

Derek Vanditmars, Delta Controls, Surrey, BC, Canada

Adding a manual reset to a design usually involves designing in a new part with a manual-reset input. But, by adding a couple of low-value resistors, a standard three-pin-reset supervisor can work in most applications. The circuit in **Figure 1** ensures a clean $\overline{RESET}$ signal during and after you have pressed the manual-reset button. When you activate the manual-reset button, the supply voltage drops below the reset supervisor's minimum reset threshold because of the R_1/R_2 voltage divider formed when S_1 is active. This action causes the reset supervisor to activate its $\overline{RESET}$ output. When you realease S_1, the supply voltage returns to above the reset-supervisor maximum-reset threshold, and $\overline{RESET}$ remains active for the time-out period of the reset supervisor.

When you do not press S_1, R_2 has a voltage drop arising from the reset supervisor's supply current and $\overline{RESET}$ output loading. For most reset supervisors, the maximum supply current is 50 μA. For most designs, the $\overline{RESET}$ output goes to one or more CMOS inputs that require about 10 μA each. With two CMOS devices connected to $\overline{RESET}$, the total current through R_2 would be (2×10 μA)+50 μA=70 μA. The voltage drop across R_2 due to the current flow effectively adds 70 μA×100Ω=7 mV to the reset su-

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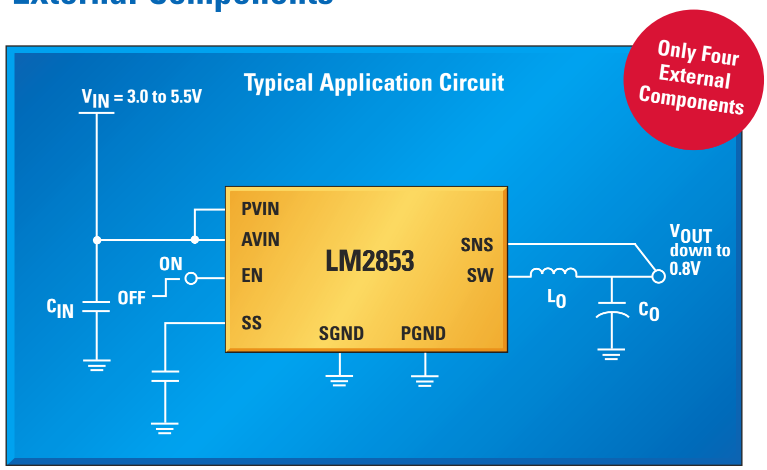

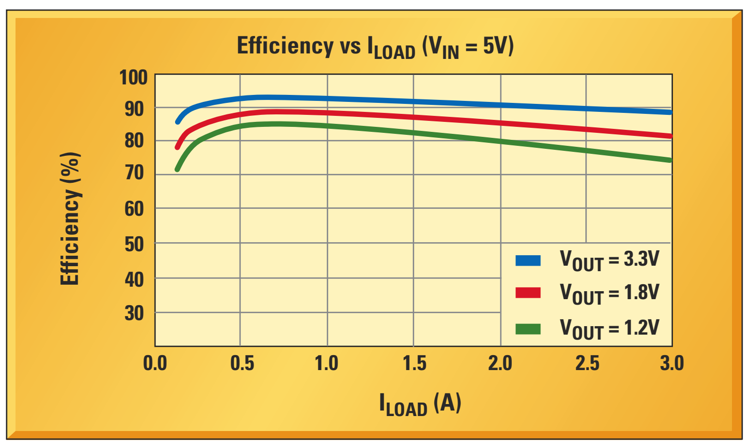

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LM2852	2.85 to 5.5	2A	500 kHz or 1.5 MHz	0.8V to 3.3V	eTSSOP-14
LM3100	4.5 to 36	1.5A	Programmable up to 1MHz	Adjustable from 0.8V to 90% V_{IN}	eTSSOP-20

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pervisor's reset-threshold voltage.

You should consider several tradeoffs for the selection of values for R_1, R_2, and C_1. The value of the local bypass capacitor, C_1, for the reset supervisor should be low enough to allow the reset supervisor to detect transient supply-voltage drops. The time constant of R_2 and C_1 determines this factor; in this example, the time constant is $100\Omega\times0.01\ \mu F=1\ \mu sec$. This figure is typically much higher than the decay rate of a regulated power supply that has lost power.

When you activate S_1, current flows through R_1 and R_2. In the circuit in **Figure 1**, the current flow when you activate S_1 is $3.3V/(100\Omega+100\Omega)=16.5$ mA. This amount of current would be OK for a line-powered system but may not be OK for a battery-powered system. You can reduce the current by increasing the value of R_1 and ensuring that the reset supervisor's supply voltage drops below the minimum reset threshold. You can also increase the value of R_2, along with that of R_1, but doing so will cause increased voltage drop and slower response to transients. Note that the increased current of the manual reset occurs only while the manual reset is active, and typical system current drops while $\overline{\text{RESET}}$ is active. **EDN**

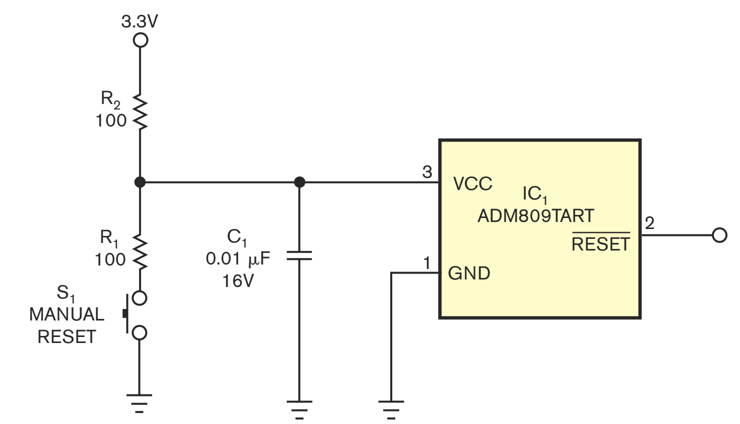


Figure 1 A pair of low-value resistors, a capacitor, and a pushbutton add a manual-reset function to a standard three-pin-reset supervisor.

productroundup

CIRCUIT PROTECTION

Electronic-circuit protector uses selective disconnection to minimize system disruption

Allowing selective disconnection of loads connected to 24V-dc switch-mode power supplies, the ESX10 electronic-circuit protector features selective load protection. This feature prevents complete shutdown of the system by disconnecting the faulty path during an overload or short circuit. Limiting the maximum current to 1.3 to 1.8 times the rated capacity allows switching on capacitive loads as large as 20,000 μF, disconnecting only during an overload or short circuit. During detection of an overload or short circuit in the load circuit, the power-MOSFET switching output of the device interrupts the current flow. A multicolor LED and status output signal provide a failure and status indication. Measuring 2.76×0.5 in., the protectors come in 1, 2, 3, 4, 6, 8, 10, and 12A fixed-current ratings. The ESX10 electronic-circuit protector costs $40.

E-T-A Circuit Breakers, www.e-t-a.com

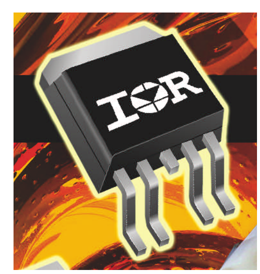
Circuit protectors guard against overcurrent and overtemperture damage

Providing protection for electric motors and transformers suiting commercial and home appliances, the Polyswitch LVR resettable circuit-protection series protects against mechanical overloads, overheating, stall, and lost neutral conditions. The components feature 120 and 240V-ac line voltages at an operating current as high as 2A at 20°C. The device does not require replacement after a fault event and restores to normal operating condition after eliminating the overcurrent condition and removal of power. The vendor claims that the device has greater flexibility, longer life span, and a lower EMI (electromagnetic interference) than bimetal breakers. The devices also prevent damage in which faults cause a rise in temperature with a slight increase in current draw. When close to magnetics, FETs, or power resistors, the product provides overcurrent and overtemperature protection with a single installed component. The LVR075S costs 25.4 cents.

Raychem Circuit Protection, www.circuitprotection.com

Intelligent power switch features reverse-battery protection

The fully protected IPS6011 high-side intelligent power switch features an integrated charge pump, allowing the switch to operate in high-side topologies without additional components. Features include a 14-mV maximum on-resistance, a 37V minimum clamp voltage, and a 60A typical overcurrent limitation. The switch also features reverse-battery protection, turning on the output MOSFET during a reverse-battery event. Targeting automotive applications, the switch aims at transmissions and gearboxes; solenoid drivers; lighting control; and brushed-dc-motor control for seats, window lifts, and wipers. The IPS6011 power switch costs $1.78 (10,000).



International Rectifier, www.irf.com

Multichannel EMI filters come in a low-profile package

Available in an LLP leadless package with a 0.6-mm profile, the four-channel VEMI45AA-HNH, the six-channel VEMI65AA-HCI, and the eight-channel VEMI85AA-HGK EMI

CIRCUIT PROTECTION

filters provide a 0.4-mm pin-to-pin pitch. Providing ESD (electrostatic-discharge) protection, the devices attenuate unwanted signals by 30 dB over 900 MHz to 2.3 GHz. Additional features include 100Ω resistance, 60-pF input capacitance, and low-leakage currents. The VEMI45AA-HNH, VEMI65AA-HCI, and VEMI85AA-HGK cost $12, $14, and $16 (100), respectively.

Vishay Intertechnology, www.vishay.com

Diode array has an ultrathin package

The NUP45V6 series of ESD (electrostatic-discharge)-protection diode arrays targets portable, wireless, and computing applications.

Providing IEC 61000-4-2 ESD performance, the series includes devices with 5.6, 6.8, and 12V protection voltages. Features include 7-pF capacitance leakage at 3V and 0.1-µA leakage current. Measuring 1×1×0.5 mm in an SOT-953 package, the NUP45V6 array costs 12 cents (10,000).

On Semiconductor, www.onsemi.com

ESD-protection device uses solid-state silicon-avalanche technology

Joining the vendor's MicroClamp ESD (electrostatic-discharge)-protection family, the uClamp0524P offers IEC 61000-4-2 protection on four lines to protect sensitive electronics from damage or latch-up from ESD, lightning, and other voltage-induced transient events. Features include a 5V working voltage; four lines of protection, replacing as many as four discrete devices; and ±15-kV-air and ±8-kV-contact ESD protection. The device uses solid-sate silicon-avalanche technology. The uClamp0524P costs 44 cents (1000).

Semtech Corp, www.semtech.com

TEST AND MEASUREMENT

UWB data-recording system allows real-time recording/playback

Suiting high-speed sensor applications, the VXS-based JazzStore UWB (ultrawideband) data-recording system uses a FAT (file-allocation-table) 32-based filing system, providing access to recorded data from Linux-, VxWorks-, or Windows-workstation environments. This disk-based data-recording device enables real-time, high-capacity recording and playback of broadband-sampled analog data at 2G samples/sec in 8-bit samples, or 1.6G samples/sec in 10-bit samples. Based on multiple RAID (redundant-array-of-inexpensive-disks) storage, the two-slot storage architecture provides enough capacity for storing wideband-sampled data for several hours. Users control the system through a Windows GUI or from software applications through an API (application-programming-interface) library. The system has a scalable capacity and uses six dual Fibre Channel RAID systems, allowing as much as 24 Tbytes of storage capacity. Available 90 days after receipt of order, the JazzStore UWB system costs $125,000.

TEK Microsystems, www.tekmicro.com

New multiple-recording option allows for radar signals

The UF2 family of 66-MHz PCI-based oscilloscope/digitizer cards adds a multiple-recording feature, aiming at recording radar signals. The option allows users to acquire a fast series of waveforms with a high repetition rate without restarting the hardware during the short dead time between waveforms. Suiting use for recording high-speed series of waveforms, including sonar, ultrasound, and laser, the multiple-recording option costs $290 and is available for 8-, 12-, 14-, and 16-bit-resolution oscilloscope PCI cards.

Strategic Test Corp, www.strategic-test.com

Test tool mixes boundary scan and functional test

The ScanExpress JET (JTAG-emulation test) combines boundary-scan and functional-test technologies. The tool incorporates common-pin and net-level diagnostics using boundary-scan testing with processor-emulation testing through the JTAG port. This feature provides test capabilities on designs using JTAG-compatible processors to non-JTAG-peripheral components, including analog parts in the processor-address and I/O space. This feature allows

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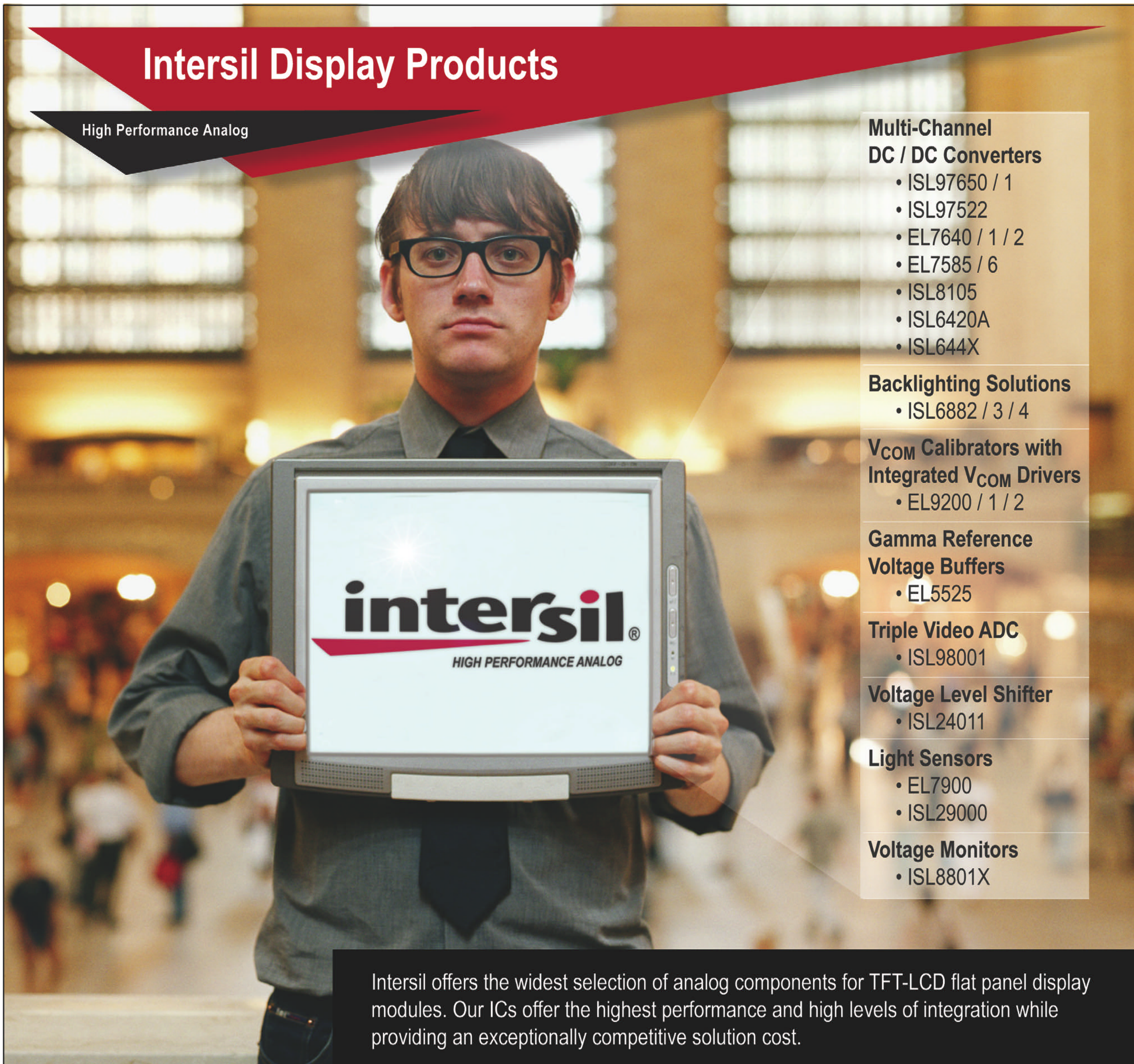

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sound structural tests for opens and shorts using boundary-scan testing and the ability to perform at-speed functional testing using the processor for running test programs loaded into memory. Before loading test programs into onboard memory, the device tests the memory at speed, without loading code into it, allowing testing and diagnosis of faulty boards and systems when the embedded processor cannot boot and the board self-test is not operating. The ScanExpress JET costs $17,000.

Corelis, www.corelis.com

MICROPROCESSORS

Microcontrollers have dual-bank flash-memory-upgrade option

Joining the ARM7TDMI processor-core-based AT91SAM7S, AT91SAM7X, and AT91SAM7XC microprocessors, the 512-kbyte AT91SAM7S512, AT91SAM7X512, and AT91SAM7XC512 dual-bank flash-memory extensions double the amount of flash memory of their predecessors. Designers can simultaneously program the dual flash memory because it is in a two-bank arrangement. Additional features include double the density of the zero-wait-state memory, 11 to 13 dedicated peripheral-DMA channels, and a 32-bit-wide SRAM on the AT91SAM7X512 and 64- to 126-kbyte AT91SAM7XC512. The devices use a hardware cryptoengine that performs 128-, 192-, or 256-bit AES (Advanced Encryption Standard) or 3DES (Triple Data Encryption Standard). The AT91SAM7S512 comes in LQFP-64 and QFN-64 green packages, and the AT91SAM7X512 and AT91SAM7XC512 come in LQFP-100 and BGA-100 green packages. The extensions are available at a 20% cost increase; the devices cost $6 (10,000).

Atmel, www.atmel.com

DSPs suit low-end- to midrange-wireless-system applications

Based on the TMS320C64x+ core, the TMS320C6424 and TMS320C6421 DSPs suit low-range to midrange wireless-system applications, including home gateways and base stations, printers, scanners, copiers, and wireless speakers. Features include 4800 million multiply/accumulate operations at 600 MHz, a 1.6- to two-times boost in raw DSP power, EDMA (Enhanced Direct Memory Access) 3.0 with 4.8-Gbps throughput and 333-MHz DDR2 memory interface, and an on-chip Ethernet media-access controller. The C6421 DSP is pin-for-pin-compatible with other C642X DSPs. The devices are upward-code-compatible with TMS320C6000 DSP platforms, and designers can program them using the vendor's eXpressDSP software. The TMS320C6424 and TMS320C6421 DSPs cost $8.95. The C6424 evaluation module, including Code Composer Studio IDE, a DSP/BIOS kernel, a chip-support library, audio codecs, and VirtualLogix's ucLinux, costs $495.

Texas Instruments, www.ti.com

Energy estimator targets Xtensa and Diamond Standard processors

Aiming at Xtensa configurable processors and Diamond Standard processors, the Xenergy energy estimator computes a power-consumption estimation per cycle for each instruction of the processor. Xenergy estimates the energy for the instruction and models the energy that all locally attached memories that are active for the instruction consume. The vendor's pipeline-accurate instruction-set simulator creates an instruction profile, which Xenergy uses to create a detailed energy-consumption profile for the user's application code. The device also includes a memory-power-consumption feature. Available as part of the vendor's software-development-kit license, the kit comes with all software-development tools, an instruction-set simulator, and the Xtensa Xplorer design environment. The Diamond Standard development kit costs $1000 per seat per year for a node-locked license; the Xtensa processor software-development kit costs $2000 per seat per year for a floating-node-tool seat.

Tensilica, **www.tensilica.com**

Microcontrollers use nanoWatt technology for low power consumption

Expanding on the vendor's 3V PIC18F J series of 8-bit microcontrollers, the PIC18F87J11 12-member family uses a nanoWatt technology, allowing 100-nA power consumption in sleep mode. Using a parallel master port for connection to external memory and displays, the family provides 8 to 128 kbytes of self-programmable flash memory with 10,000 erase-write cycles. Additional features include 5V-tolerant digital I/O, 12-MIPS performance at 3V, and an 8-MHz internal oscillator and 4× PLL providing 32-MHz operation without an external-clock source. The devices provide two SPI/I^{2}C, two UART, and five PWM communication channels. Support includes the MPLAB IDE (integrated development environment), MPLAB C18 C compiler, MPLAB ICD (in-circuit debugger), and PICDEM HPC explorer board. Available in a TQFP-64 or a TQFP-80 package, the PIC18-F87J11 costs $2.27 (10,000).

Microchip Technology, **www.microchip.com**

Ethernet-controller IC features a hard-wired TCP/IP core

Developed using the W3150A TCP/IP (Transmission Control Protocol/Internet Protocol)-stack IC, the iEthernet W5100 10/100 Ethernet-controller IC includes a hard-wired TCP/IP core and a PHY (physical-layer) interface. This memory-mapped hardware device provides low-end microcontrollers with Internet capabilities at speeds as high as 25 Mbps. WIZnet designed the W5100, which costs $5.20 (2000).

Saelig, **www.saelig.com**

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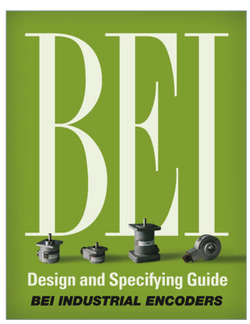

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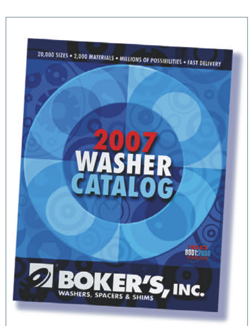

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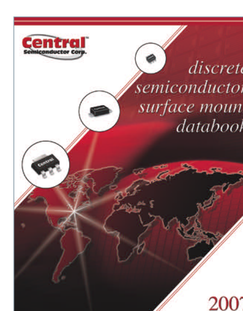

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LOOKING AHEAD

TO SID 2007

The Society for Information Display 2007 Symposium, Conference, and Exhibition, (www.sid.org/conf/sid2007/sid2007.html), the grandfather of display conferences, opens May 20 in Long Beach, CA. Once a purely technical conference about display devices and display processing systems, SID has blossomed into a complex of conferences on technical subjects, marketing, and investor information. This diversity shows in the choice of keynote speakers: a former senior vice president of Universal Pictures talking about home entertainment, a manager of display technologies at carmaker BMW Group, and a vice president from Applied Materials' display group. Technical tracks, as always, will cover almost every conceivable display technology and the electronics that support them.

LOOKING BACK

AT OPTICAL COMMUNICATIONS, VERSION 1.0

Baird-Atomic Inc has developed a light-beam communication system that can propagate single or multiple channels of voice communication or a complete television channel over a range of several miles. In a demonstration, Baird-Atomic picked up a conventional television-set display with an electro-optical system, which directed a light beam at a remotely located photomultiplier tube. The signal from the photomultiplier they fed into the video section of a second television receiver, which displayed the original picture with no loss in image quality. The electro-optical system works by projecting a constant light source through a modulator comprising a synthetic crystal plate that acts as an electro-optical shutter.
—*Electrical Design News*, April 1957

LOOKING AROUND

AT WARNINGS FROM THE CELL-PHONE MARKET

With Motorola again delivering a negative surprise to investors, even more questions are coming to light about the global cell-phone-handset market. New handset markets are often in areas such as the developing world, where extreme low cost is essential. But now it appears that even the market for midline-feature phones is growing extremely price-competitive, forcing not just price cuts, but also new architectures that can slash manufacturing costs without giving up features. Some observers suggest that this situation isn't just a fluctuation; we may be seeing the growing power of local Chinese fabless-semiconductor companies, which have targeted the feature-phone market with locally designed silicon at extremely aggressive prices.

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